High-Power GaAs FET Device Bias Considerations

The purpose of this application note is to give some general basic guidelines to bias high-power GaAs FET devices safely. However these guidelines are not a complete insurance against oscillations since each device is a unique case and its stability has to be analyzed by using standard methods if needed.

Raymond Basset
Fujitsu Compound Semiconductor, Inc.
2355 Zanker Rd., San Jose, CA 95131
(408) 232-9600
www.fcsi.fujitsu.com

While considerable effort is spent by the semiconductor companies on characterizing high-power GaAs FET devices in RF and how to match them, little effort is spent for the bias techniques. Experience shows that a lot of amplifier designers spend significant time trying to solve stability problems. These problems are due to the fact that high-power devices have very large gate periphery and consequently large transconductance. Several issues specific to high-power devices have to be addressed for the design of the bias circuits and for the turn-on and –off sequences of these devices.

Turn-on and turn-off biasing sequences

During the turn-on and -off of the devices, precautions have to be taken to avoid oscillations and device transient burnout. The limits defined in the device data sheet have to be respected. The below sequences prevent exceeding these limits and minimize the probability of oscillations.

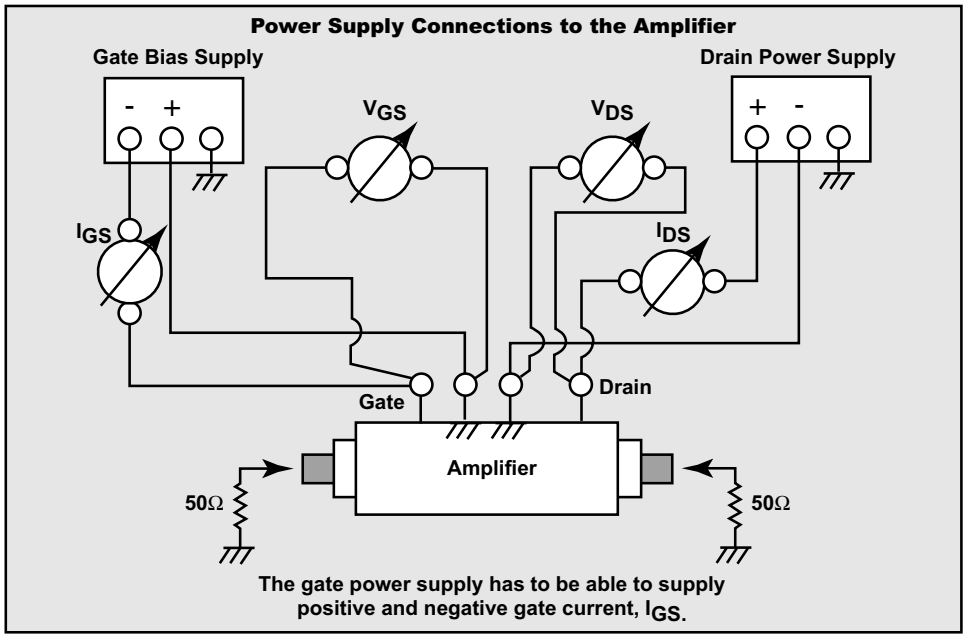

Figure 1. Power Supply Connections to the Amplifier

Turn-on procedure:

1. All test equipment, tools, and operator should be properly grounded and the input and output of the amplifier connectors connected to a 50-ohm load.
2. Regulated power supplies are recommended.
3. Adequate voltage spike protection on both bias lines is recommended.
4. Apply 0 V on the gate, Vgs=0 V, and on the drain, Vds=0 V.
5. Decrease Vgs down to the minimum device pinch-off voltage, Vgs=VpMin. Please note that Vp is an algebraic number. It should be about –4 to –0.5 V depending on the device.
6. Slowly increase Vds up to the recommended Vds value. It should be 10 or 12 V.
7. Increase Vgs to obtain the recommended quiescent drain current, Idsq.
8. Apply RF drive.

Turn-off procedure

1. Turn off the RF drive.
2. Decrease Vgs down to VpMin, about –4 to –0.5 V depending on the device.
3. Decrease Vds down to Vds=0 V.
4. Increase Vgs to Vgs=0 V.

Remark: Power devices are particularly unstable at low drain voltages. This is the reason why during the two sequences the device is in pinch-off when Vds is lower than the recommended operating Vds value, 10 or 12V.

Power supplies and their connections to the amplifier

Due to the very large transconductance of high-power devices, it is important to minimize any drain-to-gate coupling due to the wires used to connect the devices to the power supplies and to the ammeters and voltmeters.

The wires connecting the amplifier ground to the positive gate power supply terminal and to the negative drain power supply terminal should be independent. It means two separated wires should be used. Both of them should be connected as close as possible to the device flange (see Figure 1). The drain and the gate wires should be as far as possible from each other to minimize coupling. A better solution is to use shielded cables and ground these cables (shielding, positive gate and negative drain wires) only at the amplifier ground close to the device.

The internal resistance of the ammeters in the gate and drain bias circuits should be as low as possible even if Kelvin probes are used to measure the gate and drain voltages. As an example, the value of the gate resistance, Rg, in series with the gate has a recommended value. The total value of the resistance seen from the device gate (see Figure 2) should be the recommended value. If an ammeter is used with an internal resistance Ra, the resistance Rc connected in series in the gate bias circuit should be the recommended value Rg minus Ra. This assumes that the internal resistance of the power supply is very small.

With low drive level the gate current, Igs, is negative and has a low absolute value. Under large drive, Igs is positive with a relatively large value, up to 300 mA for large devices. It means the gate power supply has to be able to supply positive and negative currents. Standard laboratory power supplies cannot supply positive currents. In this case a resistance, Rp, has to be connected in parallel to the gate power supply terminals, (see Figure 3). Its value to insure that the internal current, I, in the power supply will flow from the negative to the positive terminal has to be:

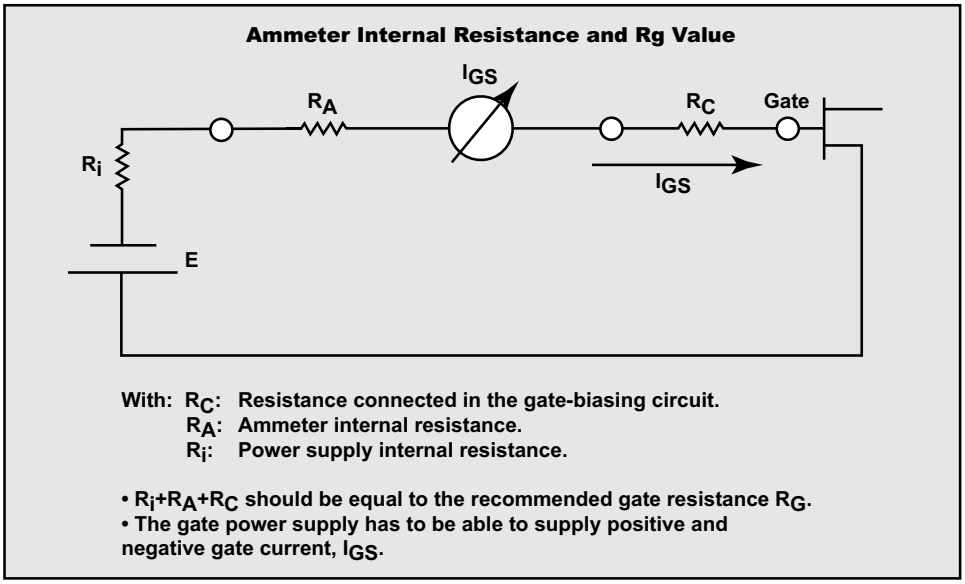

Figure 2. Gate Biasing Circuit: Gate Resistance

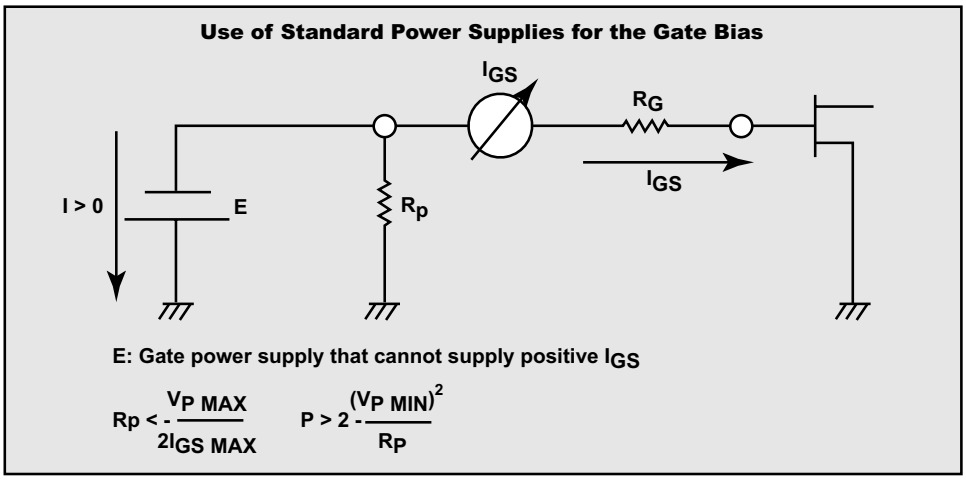

Figure 3. Use of Resistor in Parallel of the Gate Power Supply

Rp< (-VpMax)/(2IgsMax) **where**

VpMax is the maximum pinch-off voltage
Igs is the maximum gate current under drive.

It is assumed that the highest gate voltage where the device may operate is half the maximum pinch-off voltage. It is a conservative assumption.

Please note that Vp and Igs are algebraic numbers and Vp is negative and Igs here is positive. As an example, if an FLL1500IU-2C device is used, VpMax=-0.1 V and if IgsMax=60 mA for the application:

Rp<0.1/(2x0.060)= 0.8 ohm

The power rating of this resistance should be:

Pr> (VpMin)²/Rp **where**

VpMin is the minimum pinch-off voltage of the device.

Because Vgs applied to the device can be lower than VpMin, a resistance with at least a power double of this minimum power should be used.

For the present example, FLL1500IU-2C, Rp<0.8 ohm and VpMin.=-0.5 V, the resistor power has to be:

Pr> 0.5²/0.8= 0.3 W

A 1-W, 0.7-ohm resistor should be connected in parallel to the terminals of the gate

power supply. That insures that a positive gate current can be supplied up to 60 mA for any Vgs<-0.05 V.

Gate Biasing Circuit

The gate biasing circuit has several functions:

• To maintain a constant gate-to-source voltage, Vgs.

• To be able to supply a negative and positive gate current, Igs.

• To protect the gate by limiting Igs when the device goes into breakdown (drain-to-gate or gate-to-source) or when the gate-to-source junction is biased with a positive voltage. These abnormal operating conditions for the devices can be due to an operator error, an overdrive, a system problem or ESDs.

• To stabilize the device in case a negative resistance appears in the gate at any frequency where the device has a positive gain.

• To filter the signal, the products and the harmonics generated by the device input from low to high frequencies without affecting the device input matching circuit.

• To isolate the gate from any signal coming from the drain through the bias circuits.

Figure 4 shows a generic amplifier block diagram. Figure 5 illustrates a circuit used when the biasing circuit has no matching function. In this case the gate resistance is placed as close as possible to the device gate for better protection again ESDs and oscillations. The impedance of this circuit in parallel to the input matching circuit is infinite at the fundamental frequency (assuming the circuit losses are low). The characteristic impedance of the first short-circuited quarter-wavelength line can be relatively large since the gate current is low. Figure 6 exemplifies a biasing circuit used as parallel short-circuited stub for matching purpose. It presents an impedance Z= jZotanθ (assuming the losses are low) connected in parallel to the input matching circuit. In this case Rg cannot be connected between the input matching circuit and the bias circuit. It is connected between the extremity of the first microstrip line and C_2 capacitor. It is important for the protection of the gate that Rg is connected before the large capacitor C_2. The capacitor C_1 has a low value since it resonates at the fundamental frequency (that includes the via hole inductance to the ground), cannot store too much energy and has high impedance for the low frequencies. It means for low frequencies if a negative resistance appears in the gate, it will be in series wit Rg and the total resistance value should be positive.

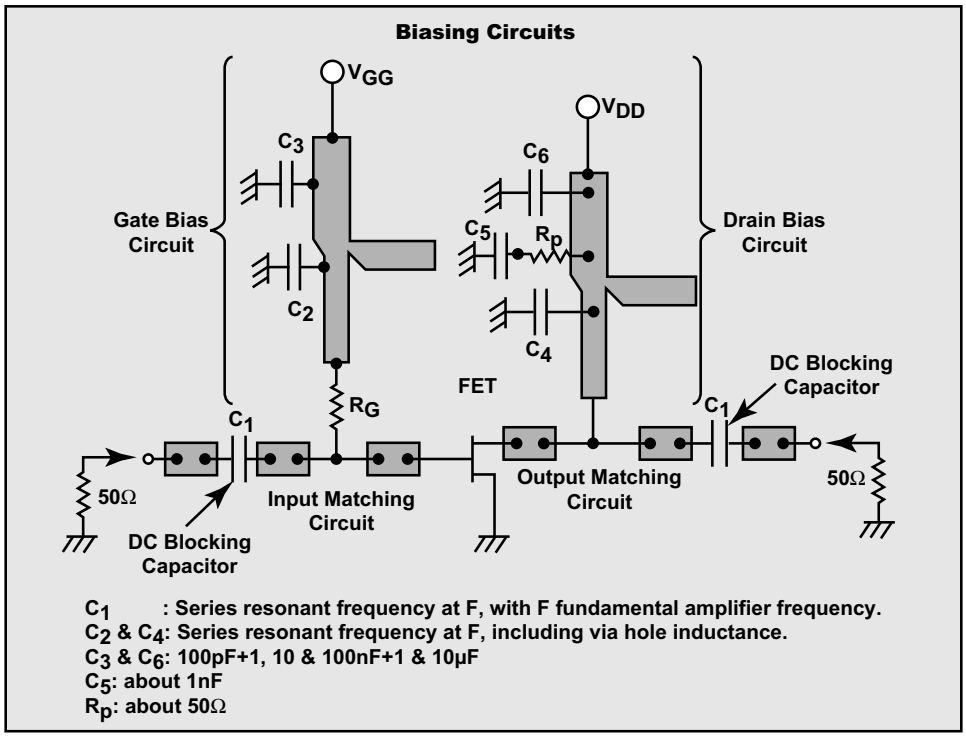

Figure 4. Amplifier Block Diagram

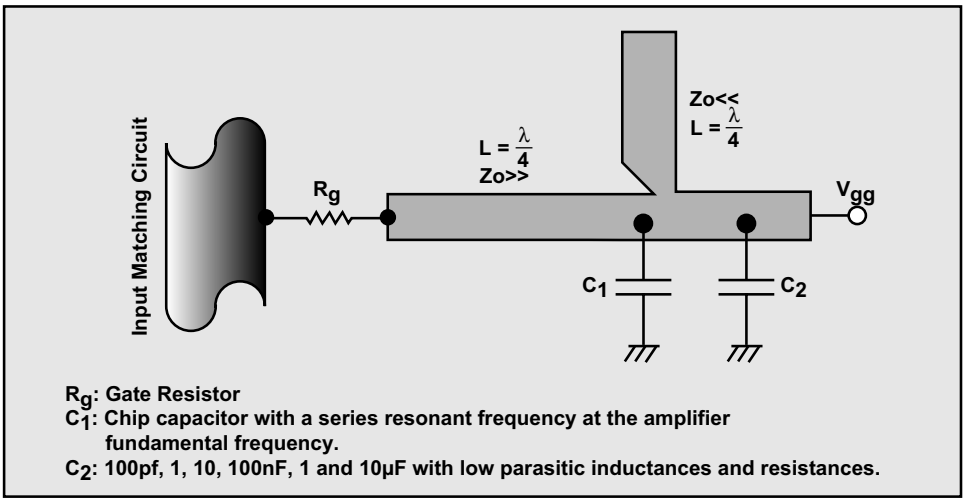

Figure 5. Gate Bias Circuit

It should be noted that the capacitor C_1 is not needed when an open-circuited quarter-wavelength low impedance line is used since the line input impedance is null at the fundamental frequency.

Rg Minimum Value

• For low frequency stability the gate resistor should be connected as close as possible to the gate. For these frequencies, the DC blocking capacitor is an open circuit, the decoupling capacitors are short circuits and the quarter-wavelength line is a very short electrical length. If a negative resistance (R<0) appears in the gate and the sum of the resistances is positive (R+Rg>0), the device will be stable. It requires Rg to have a sufficient value and the connection to the ground to be short for low frequencies. Connecting Rg close to the gate reduces the connection length to the ground.

• The gate current limitation under breakdown, positive voltage, large drive and ESDs requires a sufficient Rg value but this value for the below reasons has to be limited.

Rg Maximum Value

• The gate voltage, Vgs, should be maintained constant versus the drive level. Igs versus drive can change from a negative value to 300 mA for the largest devices. To limit the variation of Vgs, ΔVgs, versus drive,

the maximum value of Rg has to be limited:

RgMax= -ΔVgs/ΔIgsMax where

ΔVgs<0
ΔIgs=IgsMax-IgsMin

Because -IgsMin is very small, ΔIgs=IgsMax .

For an FLL1500IU-2C, IgsMax.= 60 mA at compression and if the desirable limit of ΔVgs=-0.15 V, the maximum value of the gate resistance is:

RgMax=0.15/0.060= 2.5 ohms

• The device thermal runaway limits also the maximum value of Rg. The runaway mechanism can be explained as follows: Vgs=Vgg-IgsRg, with Igs negative without RF drive. Thus when the temperature increases, Igs decreases and Vgs increases. This increase of Vgs increases Ids, which increases the power dissipated in the device i.e. the channel temperature. The channel temperature rise decreases Igs more which increases Ids and so on. The Rg maximum value to avoid thermal runaway is defined experimentally and is fortunately higher than the value already defined.

Rg Value

The value of the resistance that should see the device gate is given in the device data sheet or in the Fujitsu catalog. This resistance is called Rg but it may be different than the resistance directly connected in the gate biasing circuit. Other resistances may be involved.

If the value of Rg cannot be found, the following formula for GaAs FETs with Vds from 9 to 12 V may be used:

Rg= 400/ Psat where

Rg is the gate resistance in ohms, Psat is the output saturated power in W.

For devices called "push-pull" devices this resistance is the equivalent resistance in each gate and the output saturated power is the power of each device side.

Drain Bias Circuit

The drain bias circuit has several functions:

• To maintain a constant drain-to-source voltage

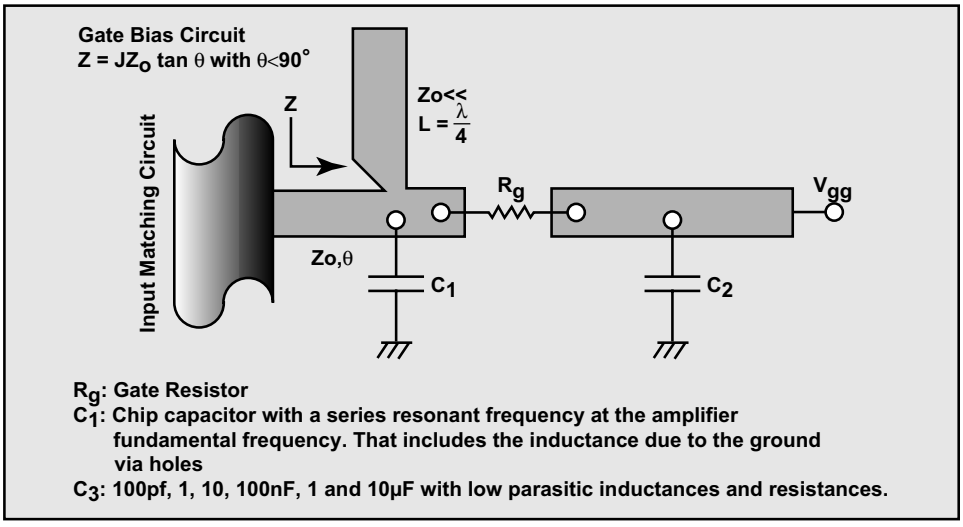

Figure 6. Gate Bias Circuit Part of the Input Matching Circuit

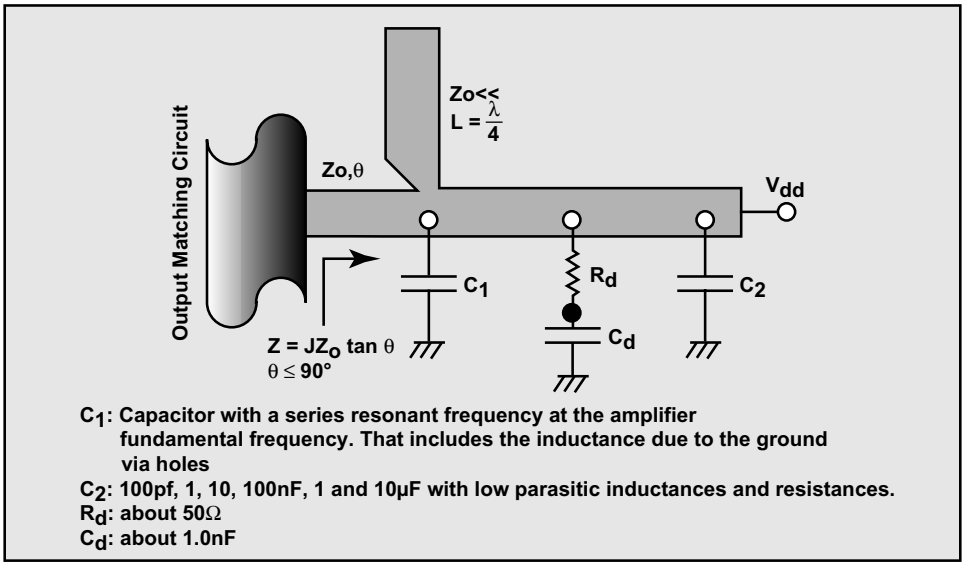

Figure 7. Drain Bias Circuit

• To supply a drain current at least up to Ids maximum under drive.

• To stabilize the device for the frequencies out of the amplifier bandwidth.

• To filter the signal, the products and harmonics generated by the device from low frequencies to high frequencies. It should be noted that as for the input biasing circuit the output biasing circuit also can be used as matching element.

• Isolate the gate from any signal from the output circuit.

Figure 4 shows the amplifier block diagram and Figure 7 exemplifies a generic amplifier drain biasing circuit. If this circuit is used as matching element, the length of the first line is shorter than 90° and the circuit presents an impedance Z= jZotanθ (assuming low losses) in parallel with the output matching circuit. If its function is only biasing, θ=90° and its impedance is infinite at the fundamental frequency.

In addition to the standard decoupling capacitors, a resistor, Rd, in series with a capacitor, Cd, is connected from the extremity of the first microstrip line to the ground. This circuit brings a dissipating element in parallel to the decoupling capacitors and improves the stability of the amplifier. The microstrip first line has to carry large drain currents, Ids, up to more than 20 A for large devices. It means its minimum width is limited and consequently its maximum characteristic impedance cannot be very high. To minimize the DC drop in the biasing circuit when it is possible, the microstrip line connected to the matching circuit should have a width as large as possible.

However its characteristic impedance has to be compatible with the amplifier band-

width and this line has to be under cut-off for the first higher order mode that appears at approximately:

$Fc=300/ [Er^{0.5}(2W+0.8h)]$ where

Fc is the cut-off frequency in GHz and W and h are the width and height of the microstrip line in mm.

For stability reasons when this circuit is used only as a biasing circuit, it should be connected as a close as possible to the device drain connections. In this case the drain is connected to the ground through a very short circuit for all frequencies and the DC voltage drop between the power supply and the drain is minimized. For high drain current such as 20 to 30 A, it can improve the amplifier efficiency and output power.

The following table gives an example of the maximum current that a microstrip line can handle versus its width, W.

The DC current is that required to raise the trace temperature 100°C on microstrip. Material is Rogers 4350, 31 mils thick, with 2 ounce copper trace (0.068 mm thick). A good solder connection to an infinite heat sink on the bottom side is assumed.

For an FLL1500IU-2C device with a total maximum current of 30 A and assuming that each side of the device has a bias circuit, the minimum line width should be 1.0 mm (15 A each side). To minimize the DC drop and have some margin, a 1.5 mm line should be used. The matching circuit between the bias circuit and the device drain connection should use lines with a wider width, W, since it has to carry DC and RF currents.

The capacitor C_1 in Figure 7 is not needed when an open-circuited quarter-wavelength low impedance line is used since its input impedance is null at the fundamental frequency.

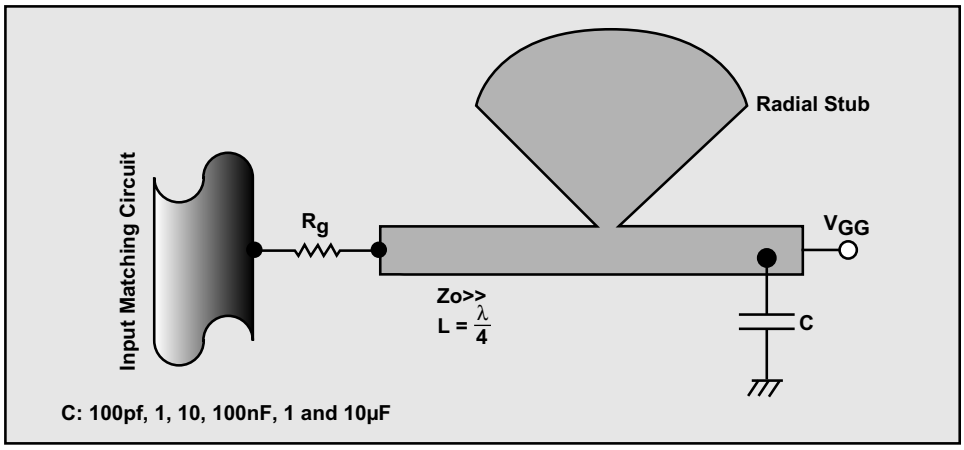

Figure 8. Input Bias Circuit using a Radial Stub

Alternative to the quarter-wavelength open-circuit stub in the gate and drain bias circuits

Instead of using in the gate and drain bias circuits a low impedance quarter-wavelength open-circuited shunt stub to realize an RF short circuit, a radial shunt stub[2,3] can be used, (see Figure 8). The advantages of using this type of stub are that it creates a low impedance to the ground at a precise point and its physical length is shorter than the equivalent transmission line.

DC Blocking Components

Several types of DC blocking elements can be used in the input and output circuits. They can also have two functions: DC blocking and RF matching. For the output circuit they have to be specially selected for their low loss and ability to handle high power. To simplify this application note only the output circuit will be considered, limited to the case of DC blocking elements with low reflection inserted in series with the output 50- or 25-ohm transmission line. Versus the frequency of the applications different elements can be used:

• At relatively low frequencies (UHF, L-& S-band) multi-layer chip capacitors may be used.

• At higher frequencies (microwave and millimeter-wave applications) single layer ceramic capacitors may be used for thin film hybrid circuits.

• Coupled lines can be used at relatively high frequencies (F>3.0 GHz) where quarter-wavelength lines have acceptable physical length. They are cheap, low loss and do not require any assembly.

Example: 2.11-2.14 GHz, 150-W balanced amplifier[4] using an FLL1500IU-2C device (Push-Pull device)

For L- and S-band applications, where plastic boards are used, often chip multi-layer capacitors in small cases are mounted in series with the input and output circuits to block the DC. For simplification, only the output circuit will be considered and it will be assumed that the capacitor is mounted in series in the 50-ohm output line.

It is desirable this capacitor have an impedance very low in comparison to 50-ohm load. So a capacitor with a resonant series frequency near Fs=2.14 GHz should be selected. As example a capacitor ATC 100 A from American Technical Ceramics, (ATC) with a 20 pF value resonates at 2.0 GHz.

ATC gives the capacitor series resistance, Rs, at 1.0 GHz, which is Rs=0.15 ohm for this value of capacitor. The value of the series resistance can be calculated at 2.14 GHz with the formula:

$R_{SF2}=R_{SF1}(F2/F1)^{0.5}=0.15(2.14/1.0)^{0.5}$ =0.22 ohm (skin effect)

The capacitor impedance at 2.14 GHz is Z=0.22 ohm, which is very low in comparison

Table 1: DC Current Handling Capacity of a 2 oz Copper (0.068 mm thick) microstrip line[1]

Width in mm	DC Current Maximum (A)
0.25	4.5
0.50	9.0
1.00	18.0
2.00	36.0
3.00	54.0
4.00	72.0
5.00	89.0

to a 50-ohm impedance. Its insertion will not affect the output matching significantly.

Its insertion loss in a 50-ohm line with VSWR=1:1 is:

Loss=20log [(2R+Rs)/2R] where

R=50 ohms and Rs=0.22 ohm

Loss=0.019 dB

Its power dissipated is:

Pdiss= Pout(Rs/R) where

Pout is half the output power of the push-pull device since each side of the device has a separated bias and matching circuit. Note that in this example the device is used in balanced configuration and 50-ohm quadrature couplers are used.

Pdiss= 75x0.22/50=0.33 W

ATC gives the thermal resistance and the maximum capacitor recommended temperature:

Rth=11.4°C/W and Tmax=125°C

In the present case and for an amplifier temperature of 70°C, the temperature of the capacitor is:

Tc=70+11.4x0.33=74°C which is lower than the maximum recommended temperature by ATC.

This DC blocking capacitor introduces a negligible insertion loss and its temperature is lower than the maximum recommended one.

DC Blocking Elements using Coupled Transmission Lines

Microstrip DC blocks (see Figure 9) are a good alternative to lump capacitors. They are easy to integrate to the amplifier layout and are nearly free. However at low frequencies, (UHF, L- and low S-band, applications) they require too much space. Their length is approximately a quarter wavelength. They can work at least a one octave bandwidth, which is more than what is needed for commercial applications considered here.

For more details see references[5].

Push-Pull Biasing Circuits

Often Push-Pull, P-P, devices, have no transversal internal connections, (see Figure10). It means the two sides of the devices are independent and can be combined in many ways as two single-ended devices: quadrature couplers, baluns and in-phase couplers. However real P-P devices, (see Figure 11), can be used only in P-P amplifiers since they have internal transversal connections between their two sides that use the virtual ground created by this configuration. This virtual ground does not exist with the other configurations. For simplicity, in this application note only bias circuits that do not use the virtual ground of the P-P configuration will be considered because they are more universal. Each side of a P-P device has the same bias circuits as a single-ended one, (see Figure 12).

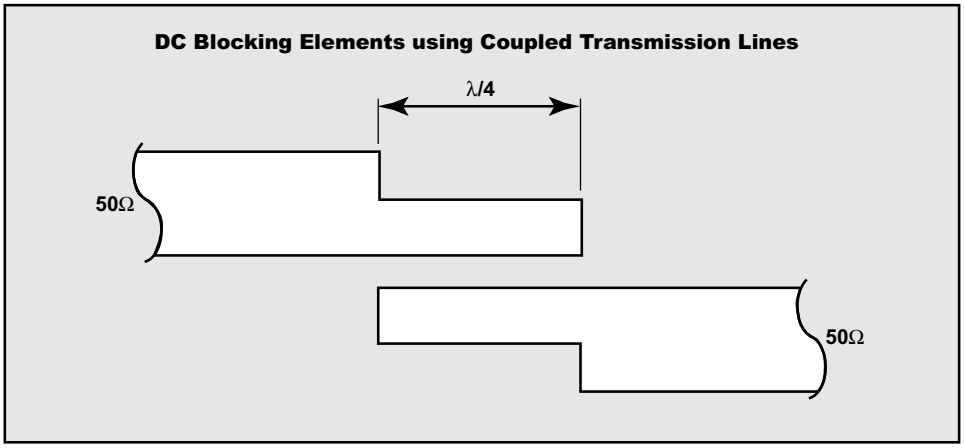

Figure 9. Coupled Microstrip Transmission Line DC Block

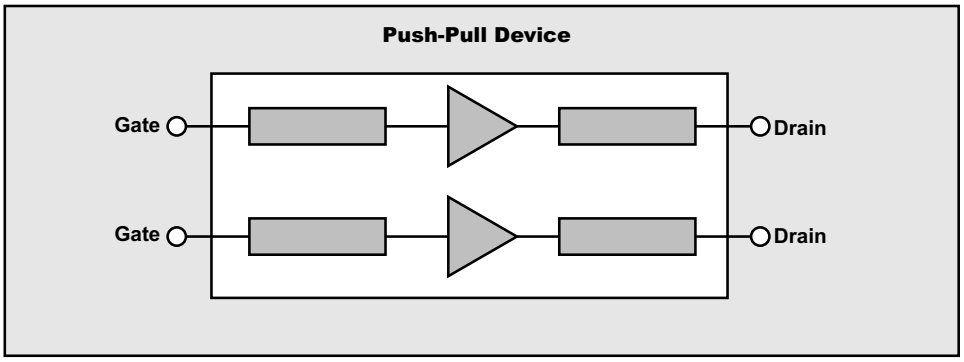

Figure 10. Push-Pull Device without Transversal Connections

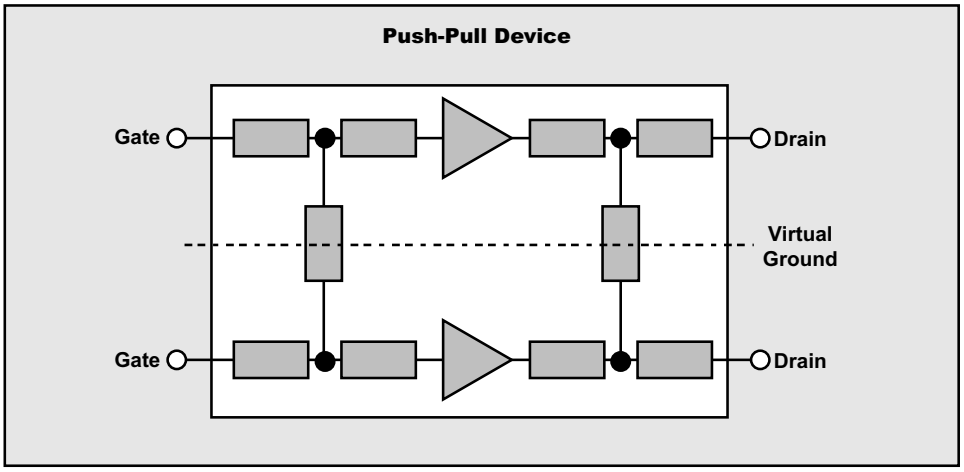

Figure 11. Real Push-Pull Device

It means a P-P device has two gate bias circuits and two drain bias circuits. Due to the fact that the chips used in a P-P device are matched, the two gate bias circuits may be connected in parallel to a single voltage source without creating a quiescent drain current unbalance between the two sides of the device. The total quiescent drain current, Idsq, is tuned by using the single gate voltage source. It should be noted that the resistance seen by each gate including the internal resistance of the voltage source, R_{IN}, should

be equal to the recommended gate resistance, R_G, of the device in the data sheet or in the catalog: $R_G=R_C+2R_{IN}$ where R_C is the resistance connected in each gate, (see Figure 13).

Biasing Condition Limits

The device data sheet gives the absolute maximum ratings for a flange temperature of 25°C and also gives the recommended Vds, Igs and the channel temperature, Tch, for a reliable operation. Tch can be calculated from the device thermal resistance given in the device data sheet with the formula:

Tch=Tf+PdissRth where:

Tch is the channel temperature in°C
Tf is the device flange temperature in°C
Rth is the device thermal resistance in °C/W in the application conditions.

Pdiss is the power dissipated in the device in W

Pdiss=VdsIds+Pin-Pout with RF and Pdiss=VdsIdsq without RF.

Thermal resistances given in the data sheet are only valid in the data sheet test conditions since GaAs material thermal conductivity is a strong function of the temperature. It means the data sheet gives Rth for a defined flange temperature, Tf1, and a defined Tch1 or power dissipated, Pdiss1. For a different set of conditions (Tf2, Tch2 or Pdiss2), the new thermal resistance, Rth2, can be calculated by using the methodology described in Microwave & RF[6] issue of October 2000. ••

References

1. Table 1 is based on MWI.EXE written by Dr. G. R. Traut of Rogers corporation. The program is available for download from www.rogers-corp.com.

2. B. Wadell, "Transmission Line Design Handbook", 1991 Artech house Boston.London, p. 300-305.

3. H. Atwater, "The design of the Radial Line Stub: A Useful Microstrip Circuit Element", Microwave Journal, November 1985, p. 149-156.

4. J. Shumaker, "High-Power GaAs FET Amplifiers: Push-Pull versus Balanced Configurations Example: W-CDMA (2.11-2.17 GHz), 150-W Amplifiers", Wireless Symposium, 12-16 February 2001, San Jose, California.

5. D. Kajfez, "Design Equations for Symmetric Microstrip DC Block", IEEE Transactions on MTT, Vol. MTT-28, No. 9, September 1980, p. 974-981.

6. R. Basset, "Understanding Thermal Basics For Microwave Power Devices", Microwave & RF, October 2000, p.101-110.

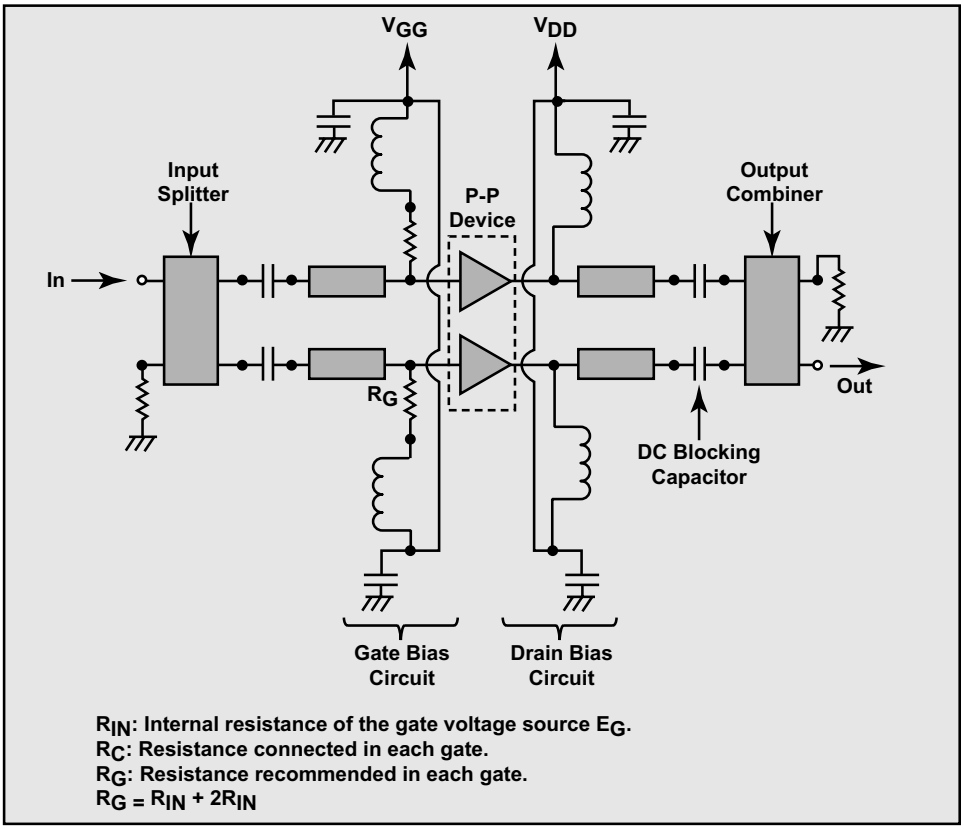

Figure 12. Push-Pull Device Block Diagram

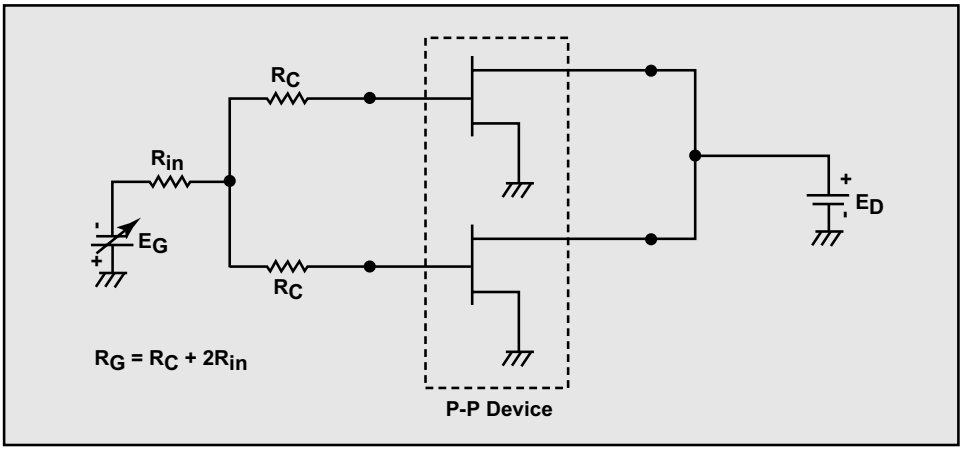

Figure 13. Push-Pull Device Gate Resistance