Reliability test report of mounting temperature cycling for WLCSP

This report describes the test results of Wafer Level Chip Size Package (WLCSP) for long-term reliability of temperature cycling after WLCSP installation on the Print Wiring Board (PWB).

Representative of device type: Daisy chain chip of WLCSP

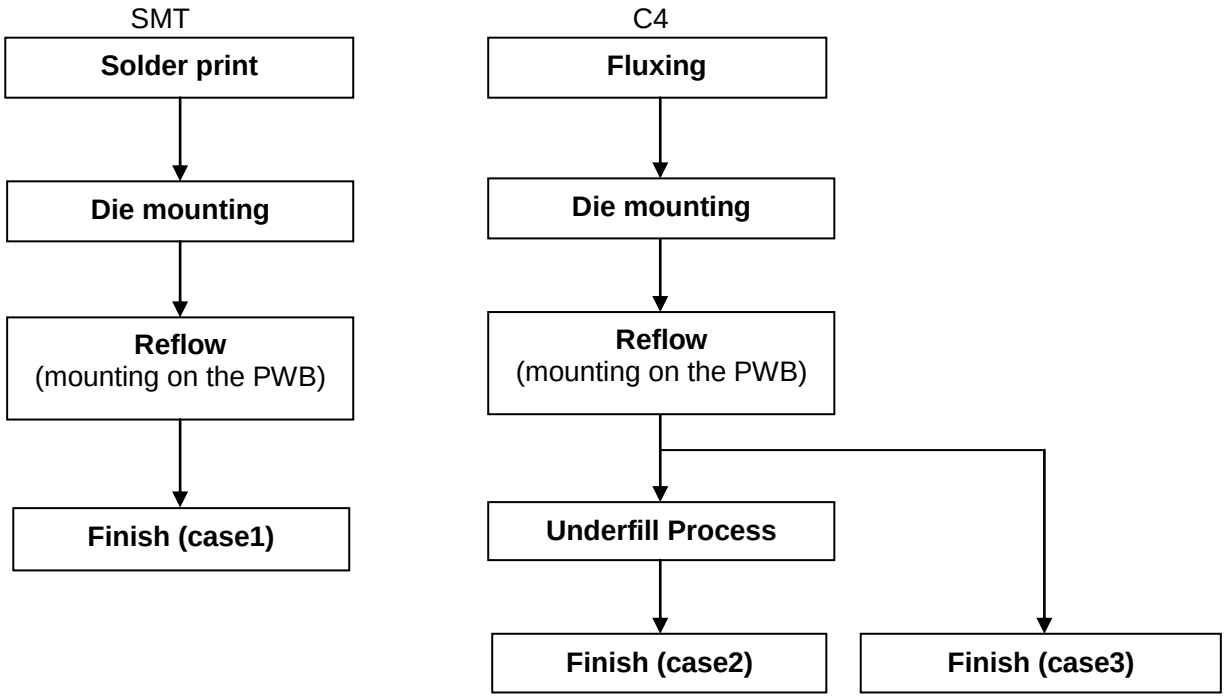
Subject of device type: WLCSP MMIC

1. Mounting condition

1.1 Flow of mounting

This section presents two flows of the WLCSP MMIC mounting on the PWB.

One is a SMT process flow with Solder print. WLCSP MMIC can be handled as a standard SMT component in the following solder print flow.
Another can also make use of C4 (Controlled Collapse Chip Connection) assembly techniques.
In this case, lower residue flux is recommended to save cleaning process step as liquid cleaning is not recommended.



Case1 – Standard SMT process flow with solder print. A stencil mask is used for solder print.
Case2 – C4 process flow with Fluxing. There is underfill step.
Case3 – C4 process flow with Fluxing. There is no underfill step.

Fig.1 Flow of mounting on the PWB

1.2 Daisy chain sample:
Fig.2 shows a daisy chain die. Fig.3 shows a PWB.

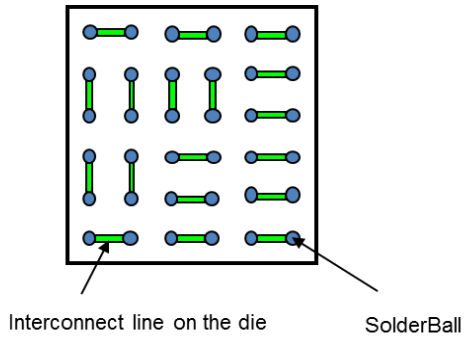


Fig.2 daisy chain die

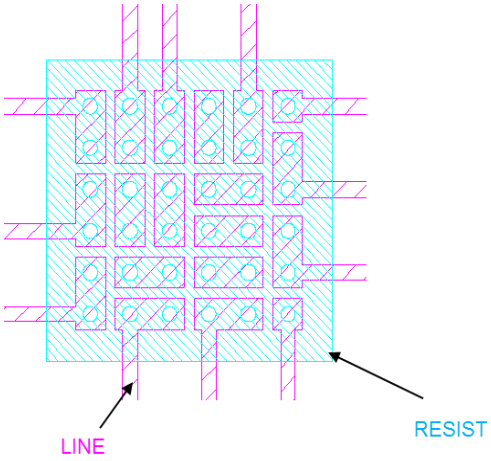


Fig.3 PWB pattern

A daisy chain die is mounted on a PWB as show Fig.4 and Fig.5. Interconnect line on the die and PWB LINE are connected in series by the solder ball.

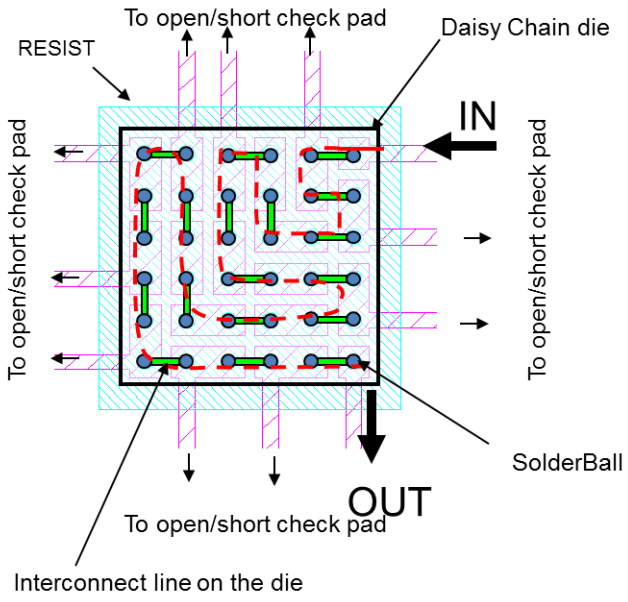


Fig.4 daisy chain sample

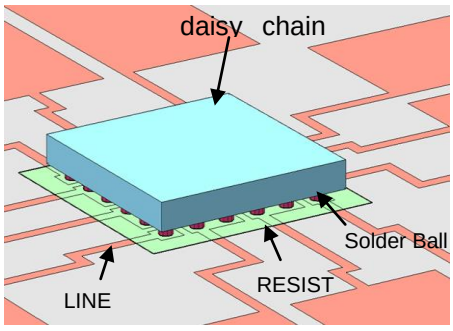
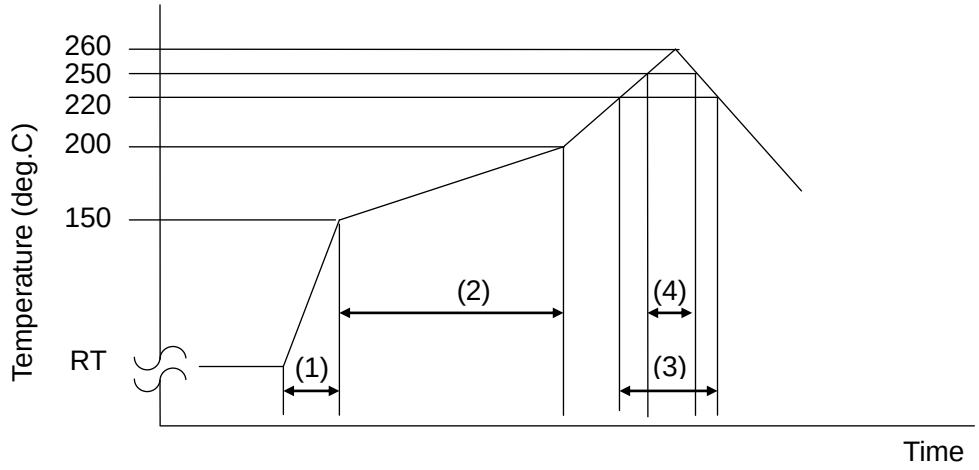


Fig.5 daisy chain sample image

Due to the variety of mounting machines and parameters and surface mount processes vary from company to company , we can supply a daisy chain die to verify the customer's assembly process.

1.3 Reflow

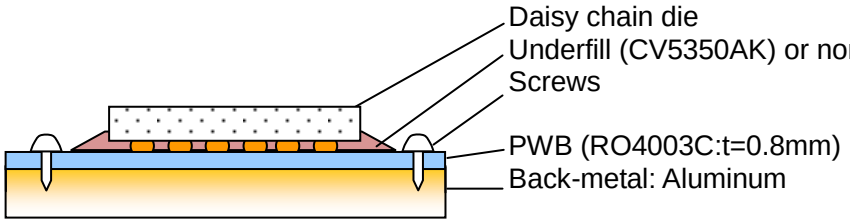
Reflow temperature profile and condition:



(1) Average Ramp-up Rate: 3 deg.C /seconds
(2) Preheating: 150 to 200 deg.C, 60 to 180 seconds
(3) Main heating: 220 deg.C, 60 seconds max.
(4) Peak Temperature: 260 deg.C max., more than 250 deg.C, 10 seconds max.

1.4 Mounting construction

The tests are performed on mounting PWB (RO4003C:t=0.2mm+Cu:t=0.5mm) using screws to attach the back metal to the PWB



1.5 Stencil mask

The stencil mask is used for solder print of 2.6mm x 2.4mm die size. The stencil mask pattern is shown in Fig. 6.

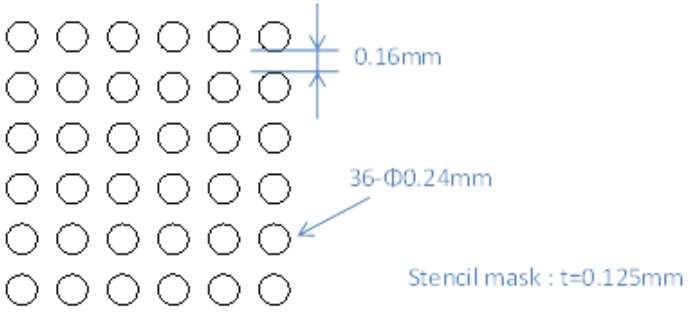


Fig.6 stencil mask

2. Mounting Temperature Cycling Test

2.1 Apparatus

(1) Temperature Cycling Test Oven:

The vapor phase type of test oven is required, which meets the test conditions of the temperature cycling profile specified in EIAJ ET-7404.

(2) The continuous electric resistance monitoring system:

During the temperature cycling test, the electrical resistance is continuously measured and automatically logged in the computer by the solder conductor resistance evaluation systems, model #AMR-040-PS with a GPIB interface manufactured by ESPEC CORP.

2.2 Failure Criterion

The failure criterion is defined when the electrical resistance increases two times the initial value. This criterion is believed to be valid for identifying failure mechanism and anomalies of solder joints. The sample was connected in a “Daisy Chain” series and monitored with the series resistance continuously.

2.3 Test Condition

Temperature Cycling Test (-40 deg.C / R.T. / +125 deg.C)

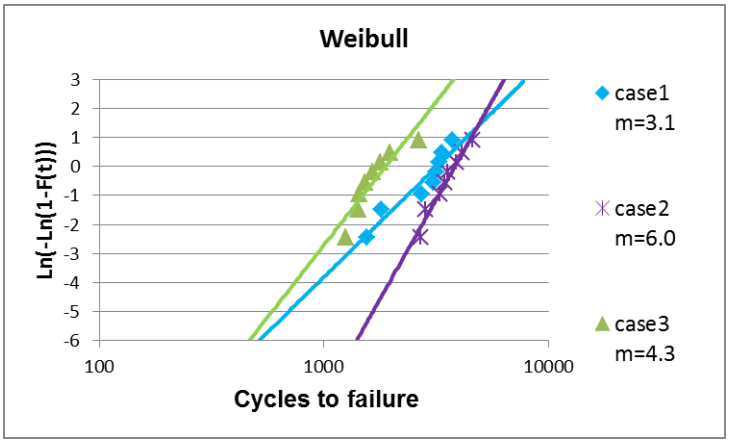
2.4 Test Results

case1 Solder print
Solder : M705-GWS-K (Senjyu Metal Industry)
Stencil mask : See p.3, Fig.6

case2 Fluxing + Underfill
Flux : DELTALUX527N (Senjyu Metal Industry)
- This is a low residue flux.

Underfill : CV5350AK (Panasonic Electric Works)
Conditions : Bake 100deg.C,1hour + 150deg.C, 1hour

case3 Fluxing + non Underfill
Flux : DELTALUX527N (Senjyu Metal Industry)
- This is a low residue flux.



F(t):Cumulative failure rate

*m : shape parameter

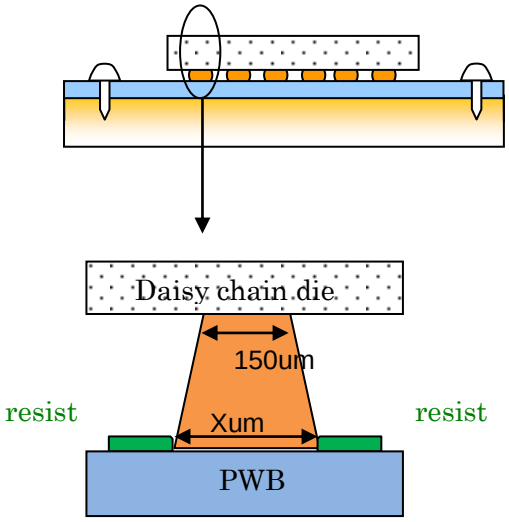
Failure mode :
Cracked solder bump

Graph1 Weibull plot

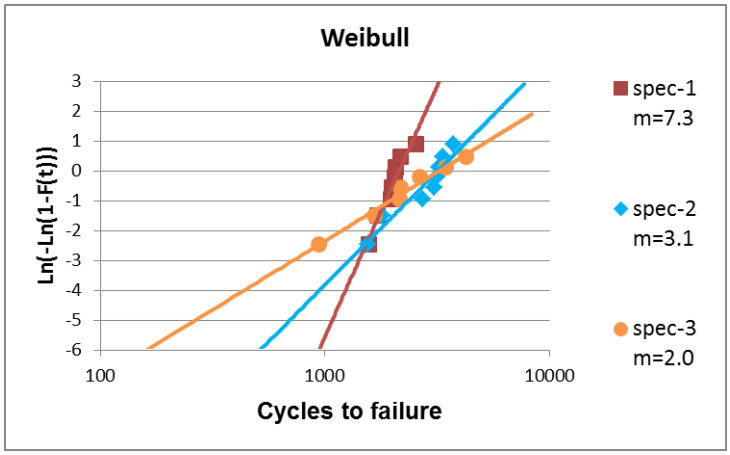
2.5 Resist window Dependence

SEDI found out the resist window dependence.

This examination applied the SMT process flow. (Solder print; case-1)



	resist window X(um)
spec-1	120
spec-2	180
spec-3	240



F(t):Cumulative failure rate

*m : shape parameter

Failure mode :
Cracked solder bump

Graph2 Weibull plot

2.6 NOTE

This information is described as reference information based on SEDI experimental test like assembly process, PWB and stencil design, Temperature cycle test result and so on.

SEDI can not guarantee the quality of WLCSP after the customer's assembly process because assembly and PWB condition is generally different between customer and SEDI.

Please check the quality of device (or system) after customer assembles with customer's PWB and assembly process.