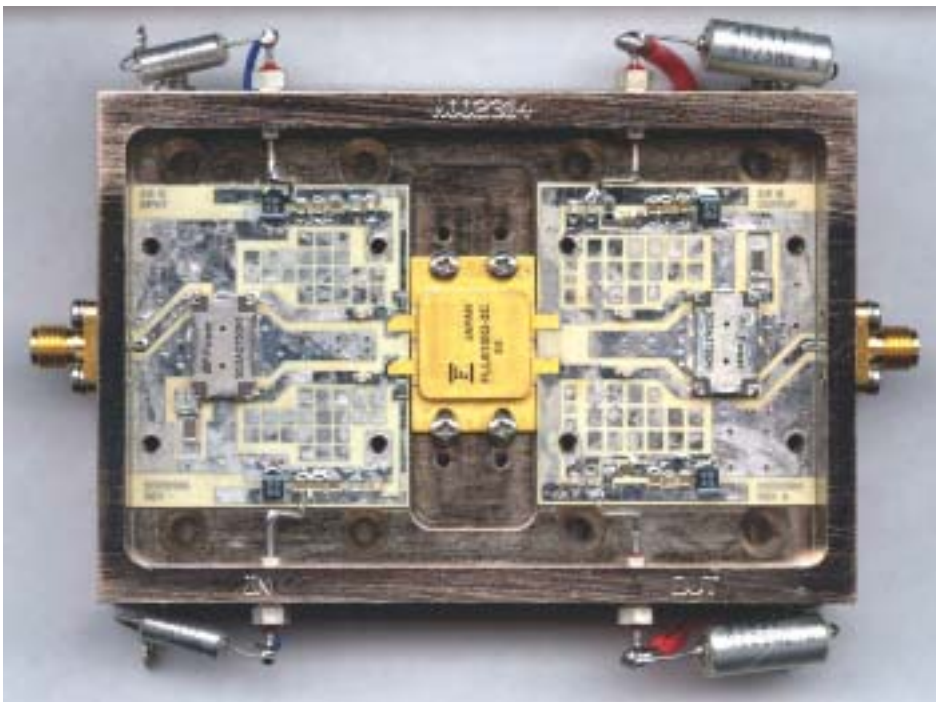


# An 80-W, 2.5-2.7 GHz GaAs FET Linear Amplifier for MMDS Application

*An 80-W, 2.5-2.7 GHz, class AB linear balanced amplifier for MMDS and wireless-data/Internet applications using a GaAs FET quasi E-mode push-pull Fujitsu device was designed. It is a compact balanced amplifier using surface-mounted quadrature hybrids. The device characterization, amplifier configuration and circuit design are discussed and the circuit layout and component list are given. Finally the averaged data of four amplifiers are reported versus frequency and output power level.*

**Jon Shumaker,  
Raymond Basset,  
& Alex Skuratov**

Fujitsu Compound Semiconductor, Inc.  
2355 Zanker Rd., San Jose, CA 95131  
(408) 232-9600  
[www.fcsi.fujitsu.com](http://www.fcsi.fujitsu.com)



## *Amplifier Features*

- Instantaneous Bandwidth:  
2.5-2.7 GHz**
- **P<sub>out</sub>: 80 W**
  - **Linear Gain: 12 dB**
  - **Gain Flatness: < 1.0 dB**
  - **Class of Operation: AB**
  - **Power-Added Efficiency: 15%  
at P<sub>out</sub>= 10 W Average  
W-CDMA signal**
  - **IM3: -36 dBc @ P<sub>out</sub>=10 W  
Average Two-Tone W-CDMA  
signal**
  - **IM3: -36 dBc @ P<sub>out</sub>=10 W  
Average Two-Tone CW signal**
  - **ACPR: -44 dBc @ P<sub>out</sub>=10 W  
Average W-CDMA signal**

**The development of Multichannel-Multipoint-Distribution-System (MMDS) and wireless-data/Internet technologies requires the use of linear and reliable high-power amplifiers in the 2.5-2.7 GHz frequency band. In opposition to the applications at lower frequencies like PCS (1.93-1.99 GHz) and IMT-2000 (2.11-2.17 GHz) ones, where the Si LDMOS FET and the GaAs FET devices are competing for power up to 240 W, at this time only GaAs FET devices are available on the market to deliver power up to 80-W in the 2.5-2.7 GHz band with good linearity and efficiency. Fujitsu has developed a new “Push-Pull” GaAs FET quasi E-mode device with an output power, Pout, of 80-W to cover a 2.5-2.7 GHz instantaneous bandwidth. The previous devices on the market were limited to 60 W. This new device was used to design an 80-W class AB compact balanced amplifier with improved linearity and efficiency at high Pout levels.**

### Design Goals

Class A or AB, 60-W push-pull devices have been available for several years.

In order to reduce the number of devices per amplifier and reduce their power supply and heat sink size, a new GaAs FET quasi E-mode was developed with Pout of 80 W to operate in class AB for better efficiency. The first goal was to fully characterize this device for the considered applications. From these parameters the second goal was to design a compact easy to produce amplifier with the target specifications given in Table 1. Since some applications use linearity correction systems that require a flat gain in a larger bandwidth than 2.5-2.7 GHz, gain flatness was targeted at better than 1.0 dB peak-to-peak for an extended bandwidth of 2.4-2.8 GHz. All other specifications apply over the 2.5-2.7 GHz bandwidth only.

### Device Description and Characterization

The FLL810IQ-3C (see data sheet in appendix I) is a push-pull device using a pair of 40-W quasi E-mode chips optimized at 12 V for higher efficiency and good linearity at high level in S-band. The chips are matched for DC and RF operation and mounted with their input and output pre-matched circuits in an IQ push-pull package. Because this device has no internal transversal connections between its two sides, no virtual ground is needed and it can be used in any amplifier configuration giving more choices to the designers.

### FLL810IQ-3C Load/Source-Pull Data

Each side of this device was first characterized with a load/source-pull automated tuner system in the 2.3-2.8 GHz band and S-parameters were measured from 1.5-3.5 GHz. The bias conditions associated with these impedances are  $V_{DS} = 12V$  and  $I_{DSQ} = 2.5A$  each side. One side (half of the device) is

measured at a time.  $Z_{in}$  and  $Z_{out}$  ( $Z_{out}|_{power}$ ) are the input and output impedances when simultaneously  $Z_{source}$  is optimized for gain, with  $Z_{load}$  optimized for output power, Pout. The impedance param-

eters converted to Touchstone compatible format are listed in Appendix II. S-parameters are also listed in appendix II. More complete S-parameters will be listed on [www.fcsi.fujitsu.com](http://www.fcsi.fujitsu.com) as they become available. The S-parameters are used to optimize the input circuit for gain and gain flatness and to analyze the amplifier stability. Table 2 shows  $Z_{in}$ ,  $Z_{out}$  and the performance of half the device versus frequency for a CW signal. Figure 1 gives the measurement methodology and the impedance definitions.

### Amplifier Configuration and Technology

#### Amplifier Configuration Choice

The FLL810-3C device allows the designer to use any amplifier configuration. Two con-

**Table 1: Target Specifications**

Flat Gain Bandwidth	2.4-2.8GHz
Linear Gain	11.5 dB
Gain Flatness (peak-to-peak)	1.0 dB
Power and Linearity Bandwidth	2.5-2.7GHz
Pout	49dBm
Power-added Efficiency, $\eta_{add}$ , for CW signal @Pout=80W	45%
$\eta_{add}$ for W-CDMA signal@Pout=40dBm Average	15%
Third-Order Intermodulation Products, IM3, Two-Tone CW signal @ Pout=40dBm Average	-35dBc
IM3 with Two-Tone W-CDMA signal@Pout=40dBm Average	-35dBc
ACPR for W-CDMA signal @ 40dBm Average Pout	-40dBc
Input and Output Return Loss	10dB

**Table 2: Single-Ended Device Impedances (Gate-to-Ground)  $Z_{in}$  and (Drain-to-Ground)  $Z_{out}$**

Freq(GHz)	$Z_{in}(Ohm)$	$Z_{out} _{power}(Ohm)$	Gain(dB)	$P_{sat}(dBm)$	$\eta_{add} \max(\%)$	IDS(mA)
2.3	47.8+j10.4	13.6+j10.2	13.7	48.4	62	8500
2.4	26.6-j5.3	16.3+j5.9	13.9	48.2	64	7913
2.5	18.4-j5.9	21.2-j5.4	13.5	48.2	59	8463
2.6	14.3+j1.7	15.7-j8.8	13.5	48.0	62	7900
2.7	10.5+j9.7	9.8-j5.0	13.1	48.3	59	8625
2.8	8.5+j16.9	6.9-j3.2	12.4	48.4	60	8775

**Table 3: Substrate Parameters**

$\epsilon_r$	h(mm)	Metallization	Metal Thickness ( $\mu m$ )
3.48	0.787	Cu	34 plated up to 68

**Table 4: Data for 90° Hybrid used in this design**

Reference	Band (GHz)	Insertion Loss(dB)	Return Loss(dB)	Isolation (dB)	Amplitude Imbalance (dB)	Phase Error (°)
RFP S03A2750N1	2.5-2.7	0.12	22	30	0.2	1.1

figurations are normally used with such devices: Push-pull and Balanced. Both balanced and push-pull configurations<sup>(1)</sup> result in a similar basic performance when operated in any class of operation and in bandwidth smaller than one octave. Both can be designed for similar linearity and efficiency performance as an amplifier for commercial application with relatively narrow bandwidth (10%). However the balanced approach has the following advantages over the push-pull one:

- Good external match allowing a direct connection of the driver to the power stage.
- Higher isolation between the two sides of the device, resulting in a better stability.
- Ease to design and integrate quadrature couplers to the amplifier.

• Better amplifier reliability: if one side is damaged the amplifier can still deliver a quarter of its original power.

For the above reasons a balanced configuration was chosen for the present amplifier.

#### Board Material

The board material selected was the Rogers 4350 for its acceptable loss, its relative dielectric constant,  $\epsilon_r=3.48$ , which allows reasonable reduction of the amplifier dimensions, and its relatively low cost. Table 3 shows the substrate properties.

#### Splitter/Combiner

For the frequencies considered, several types of quadrature couplers may be used. Examples include two-branch printed cou-

plers or surface-mounted hybrids. The latter was selected for its smaller size at the frequencies considered. Table 4 gives the basic performance of the surface-mounted hybrid in the application bandwidth.

### DC Bias Circuit Topology

#### Gate Biasing Circuit

Each side of the push-pull device has its gate and drain bias circuits. A 10-ohm gate resistor,  $R_g$ , is connected in series in each gate biasing circuit for gate protection and stability. Next is a quarter-wave length high impedance microstrip line short-circuited at its extremity by a capacitor with a series resonant frequency near 2.6 GHz. A high impedance transmission line is used due to the low gate current. See application note "High-Power GaAs FET Device Bias Considerations" number 010 for more details.

Figure 2 shows the gate biasing circuit block diagram.

Because the chips used in this device are DC matched, the two gate bias circuits may be connected in parallel to the same gate source voltage.

#### Drain Bias Circuit

The amplifier drain biasing circuit consists of a quarter-wave length microstrip line connected at one end to the output matching circuit and at the opposite end short-circuited by a capacitor with a series resonant frequency near 2.6 GHz. The quarter-wave length microstrip line is low impedance since it has to carry up to 15A maximum drain current when the device is in compression. In this design a 2.5-mm wide line is used to minimize the voltage drop in the line. Figure 3 shows the drain biasing circuit.

For more details see Fujitsu application note number 010.

#### DC Blocking Capacitors

In each input and output circuit a high quality multi-layer chip capacitor (ATC100A) with a series resonant frequency at 2.6 GHz is used as DC blocking element. Its impedance at  $f=2.6$  GHz is very low in comparison to 50-ohm impedance and its insertion loss is practically nil.

### Circuit Design

#### Design Methodology

The amplifier circuit design is performed in several steps:

- The first step is to match  $Z_{out}$  to 50-ohm impedance with a return loss better than 15

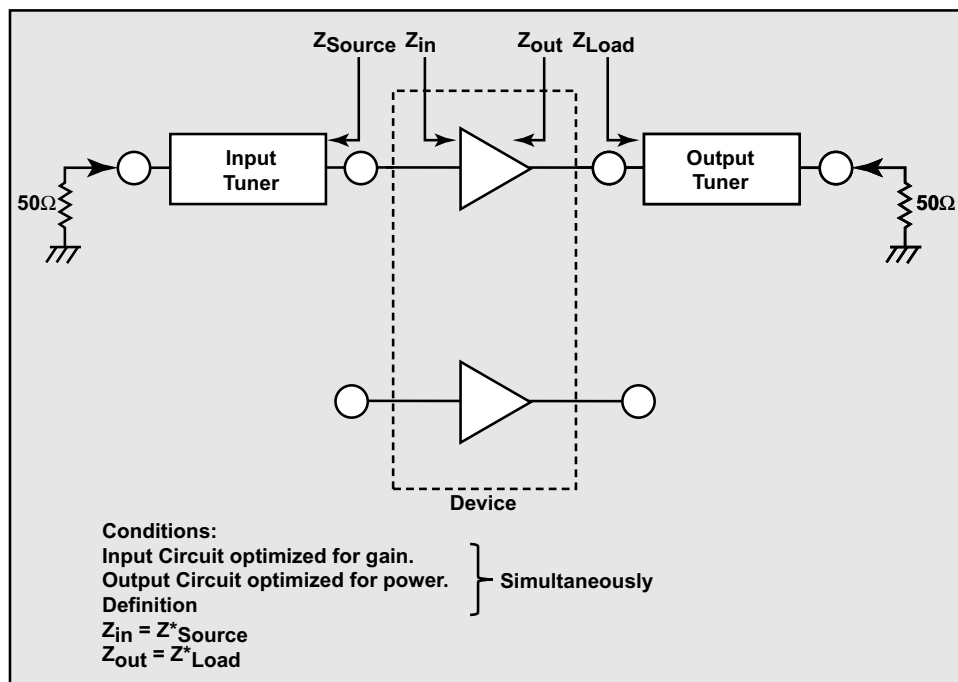


Figure 1. Source/Load-pull measurement method and definitions

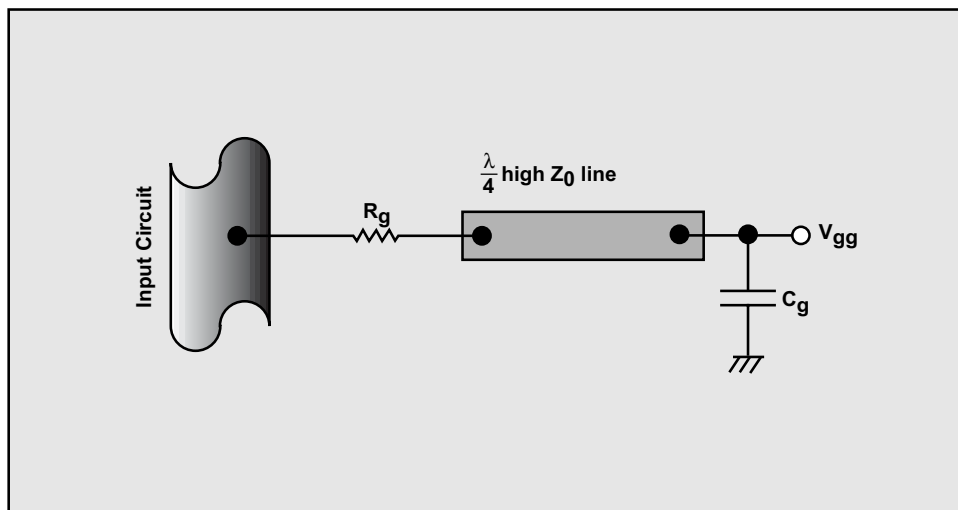


Figure 2. Gate Bias Circuit Block Diagram

dB in the bandwidth of interest. When this goal is achieved, this circuit should not be modified since no compromises should be made concerning the output power. It is assumed that  $Z_{out}$  is not significantly affected by a small change of  $Z_{source}$  during the gain and gain flatness optimization performed later.

- The second step is to match  $Z_{in}$  to 50-ohm impedance in the band of interest with a return loss better than 15 dB. This is to define the input circuit configuration and the initial values of its elements.

- The third step is to optimize the gain and gain flatness of the amplifier without the splitter/combiner that have a flat response. To accomplish this goal the S-parameters of the device are used and only the elements of the input circuit are optimized. It should be noted that the initial and final values of the input circuit elements are very close due to the fact that the gain flatness when  $Z_{in}$  and  $Z_{out}$  are matched to 50-ohm impedance is only 1.5 dB in the 2.4-2.8 GHz band, see Table 2 showing the gain versus frequency in these conditions.

- The fourth step is to analyze the amplifier stability in broadband with the S-parameters of the device. Of course it is performed without the input and output quadrature couplers.

- Finally the global amplifier small signal performance, gain and external matching, is checked in the bandwidth of interest by using the S-parameters of the device and of the quadrature couplers.

### Output Matching Circuit Design

The output matching circuit is shown in Figure 5. This circuit consists of:

- A line TL1 allowing mounting the device without cutting its drain leads.
- A line TL3 to bring the conductance,  $G$ , of the output admittance,  $Y=G+jX$ , to a value  $G=20$  mS.
- A parallel open-circuited stub, TL4, to cancel the susceptance,  $X$ , of the admittance and obtain a real impedance,  $Z=1/G=50$  ohms.
- A line TL5 (usually used to transform the real impedance,  $Z$ , to 50 ohms), since  $Z=50$  ohm simply connecting with  $Z=50$  ohm line to the combiner port.

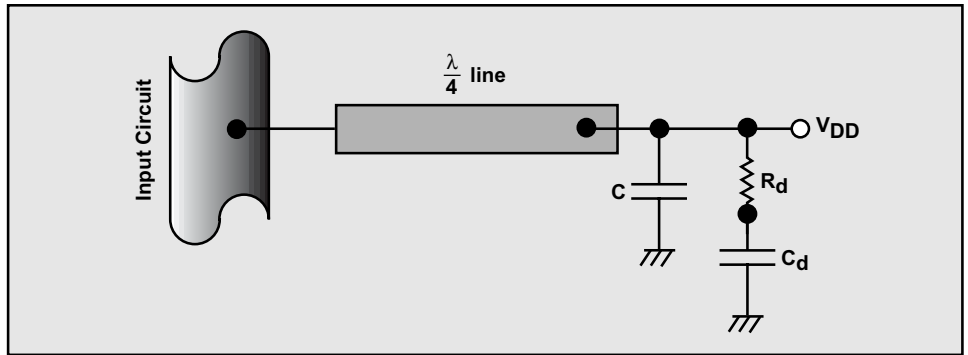


Figure 3. Drain Bias Circuit Block Diagram

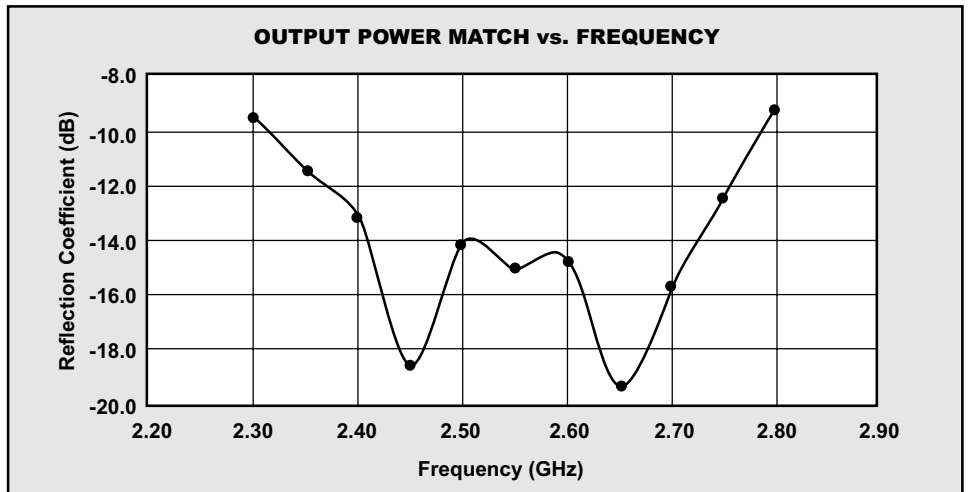


Figure 4. Output Circuit Match for Power vs. Frequency

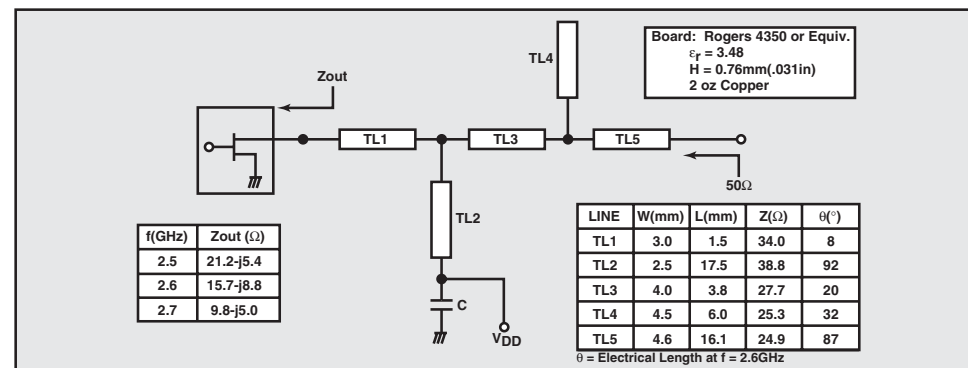


Figure 5. Simplified Output Matching Circuit for a Balanced Amplifier (2.5-2.7GHz)

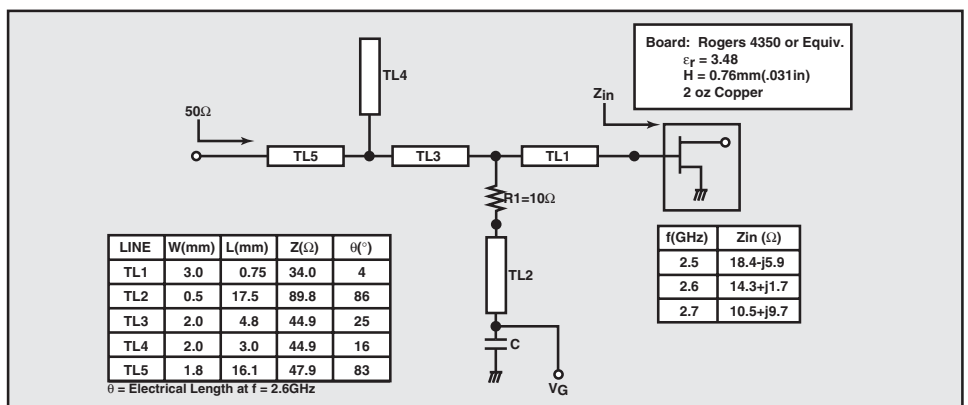


Figure 6. Simplified Input Matching Circuit for a Balanced Amplifier (2.5-2.7GHz)

- The DC blocking capacitor was placed in a convenient position in line TL5. See Figure 11.

This above explanation is a simplified one since an instantaneous band of 2.5-2.7 GHz should be covered for power.

It should be noted that the drain bias circuit (TL2 and C) has no matching function.

Figure 4 shows the magnitude of the output circuit coefficient reflection versus frequency to obtain the maximum Pout from the device in the 2.5-2.7 GHz band.

A return loss better than 14 dB was obtained in the bandwidth of interest for power, 2.5-2.7 GHz. No gain consideration was done for the optimization of this circuit since the goal was to obtain the maximum output power from the device.

### Input Matching Circuit Design

Figure 6 shows the input matching circuit for optimal gain and gain flatness. A simplified circuit description starting from the device gate is:

- A line TL1 allowing mounting the device without cutting its gate leads.

- A line TL3 to bring the conductance, G, of the input admittance,  $Y=G+jX$ , to a value  $G=40$  mS.

- A parallel open-circuited stub, TL4, to cancel the susceptance, X, of the admittance and obtain a real impedance,  $Z=1/G=25$  ohms.

- A line TL5, used to transform the real impedance,  $Z=25$  ohm to a 50-ohm impedance. See Appendix 2 for the source-pull parameters used in the design.

It should be noted that the gate bias circuit (R1, TL2 and C) has no matching function. The gate bias circuit was connected as close to the plane of the gate as possible for stability and protection purposes.

The complete single-ended amplifier circuit was analyzed using the device S-parameters measured from 1 to 4 GHz.

The amplifier input circuit was optimized for gain flatness and gain for a 2.4-2.8 GHz bandwidth. Performance was also looked at outside the band for smooth roll off. See Figure 7.

### Stability Factor

The stability of the single-ended device at relatively high frequencies was analyzed by using its S-parameters. The stability K-fac-

tor was calculated from 1 to 4 GHz and found to be greater than 1. Since the amplifier considered has no feedback, it is also unconditionally stable, see Figure 8 showing the device and amplifier K-factors. The gate resistors, drain Rd resistor/capacitor network, and decoupling capacitors should stabilize the amplifier at lower frequencies.

### Complete Amplifier Check

Two sides of the device were combined with two quadrature couplers and yielded the small signal gain and gain flatness in Figure 9A. This figure shows a predicted gain flatness better than 0.4 dB peak-to-peak and a minimum gain of 12.5 dB, exceeding both our target goals for these parameters. The magnitude of S11, S21 and S22 of the balanced amplifier in the 1.6-4.0 GHz bandwidth are shown in Figure 9B. The good external input and output match are due to

the balanced configuration of the amplifier and not to the match at small signal of the two sides of the device. This analysis was performed with the S-parameters of the device and quadrature couplers.

### Amplifier Layout

The final amplifier circuit consists of two mirror images of the input and output matching circuits, one for each side. The complete set of decoupling capacitors recommended in AN-010 was connected in the gate and drain bias circuits. As the S-parameters were measured only down to 1 GHz, modeling these capacitors with their via holes was not useful. The recommended layout for mounting the commercial couplers used was placed, along with the resistor cutout and transmission lines to the input and output circuits. The load resistor is a miniature 14-W power resistor mounted directly onto

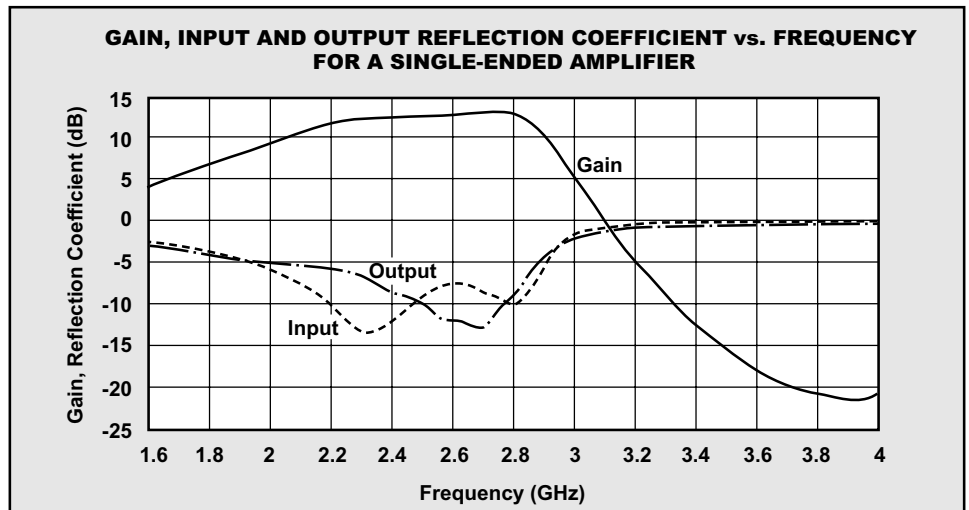


Figure 7. Gain, Input, and Output Reflection Coefficient Magnitude vs. Frequency for a Single-Ended Amplifier

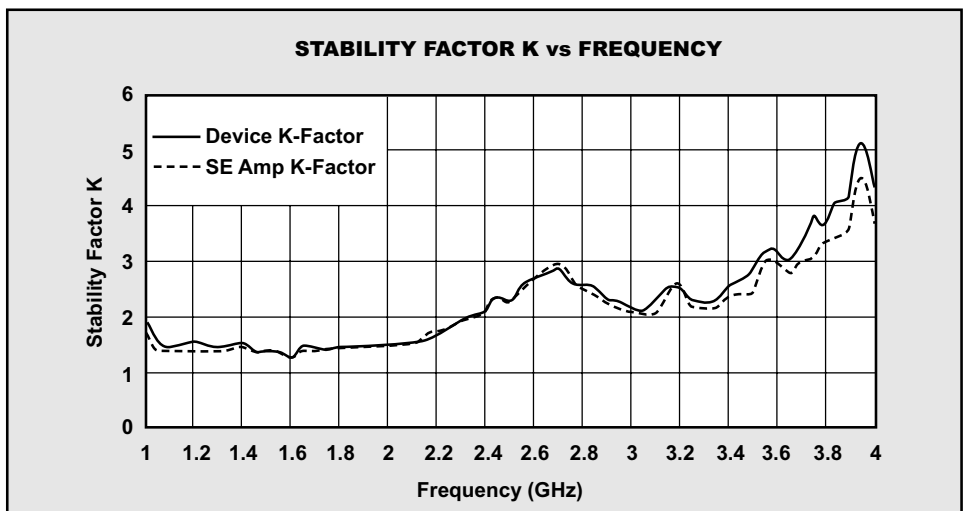
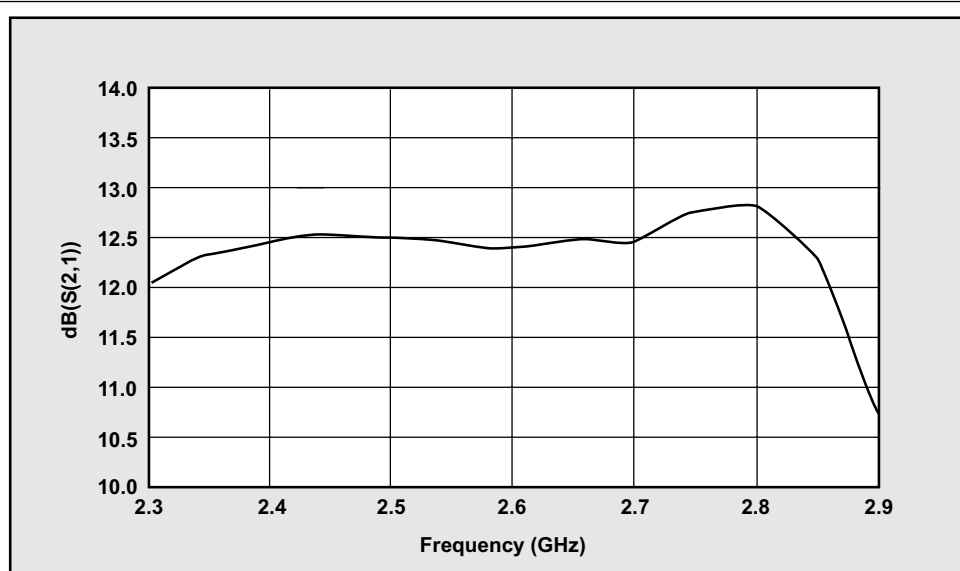
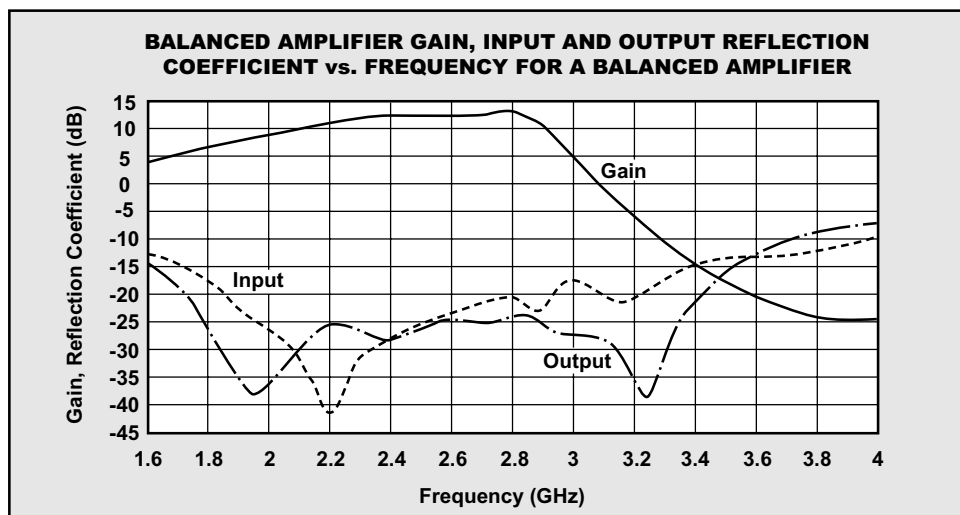


Figure 8. K-Factor vs. Frequency for the device alone and the Single-Ended Amplifier



**Figure 9A. Gain vs. Frequency for a Complete Balanced Amplifier**



**Figure 9B. Gain, Input, and Output Coefficient Reflection Magnitude for a Complete Balanced Amplifier**

the amplifier housing in a hole in the circuit board. See Figure 11 for the complete layout as tuned with parts list. The amplifier internal dimensions (boards plus device) are 95 x 44 mm<sup>2</sup>.

**Large-Signal Circuit Tuning**

The best load/source-pull data are only accurate to within about 10 percent. Therefore to obtain optimum results, some fine tuning is necessary after amplifier assembly. The FLL810IQ-3C internal pre-matching circuit made the optimization of the external circuit easy to achieve. Once the tuning was found, consistent performance was observed versus devices. Five devices were tested in the same amplifier tuned for Pout with a fixed tuning to check the consistency of the device performance. Figure 10 shows Pout versus Pin and frequency of five devices tested in one amplifier with fixed tun-

ing. The variation of Pout across the 5 samples at Pin=32 dBm is less than 0.6 dB p-p and the variation of Pout at Pin=41 dBm is less than 1.2 dB p-p.

Note that the optimal match to get Pout and power-added efficiency, η<sub>add</sub>, with a CW signal is slightly different from the optimal match for ACPR and IM3 performance with a two-tone W-CDMA signal.

Figure 11 shows the layout of the amplifier tuned for two-tone W-CDMA IM3 performance.

**Biasing and Power Dissipation Limits**

The FLL810IQ-3C data sheet (see Appendix I) gives the absolute maximum ratings for a flange temperature, Tf, of 25°C and gives also the recommended Vds, maximum

Igs, and channel temperature, Tch, for a reliable operation. Tch can be calculated from the device thermal resistance given in the device data sheet with the formula:

**Tch=Tf+RthPdiss.      where**

Tch is the channel temperature in °C  
 Tf is the flange temperature in °C.  
 Rth is the device thermal resistance in °C/W or K/W.  
 Pdiss. is the device power dissipated in W.

**Pdiss.=VdsIds+Pin-Pout      where**

Vds is the drain-to-source voltage in V,  
 Ids is the drain current in A,  
 Pin is the input power in W, and  
 Pout is the output power in W. When Pin=Pout=0 W, no RF, Ids=Idsq and Pdiss=VdsIdsq.

The thermal resistance given in the data sheet is only valid in the data sheet test conditions since GaAs material thermal conductivity is a strong function of temperature. It means the data sheet gives Rth1 for a defined set of conditions: Tf1, Tch1 or Pdiss.1. For a different set of conditions (Tf2, Tch2 or Pdiss.2), the new Rth2 can be calculated by using the methodology described in Microwave & RF<sup>(2)</sup> issue of October 2000.

For defined operating conditions, Tch can be defined and the device MTTF may be calculated by using the curve given in Figure 21.

**Example of how to calculate Rth and MTTF in a defined application**

The data sheet gives Rth1=0.8 K/W typical and 1.1 K/W maximum for Tf1=25°C and Pdiss.1=12x4=48 W.

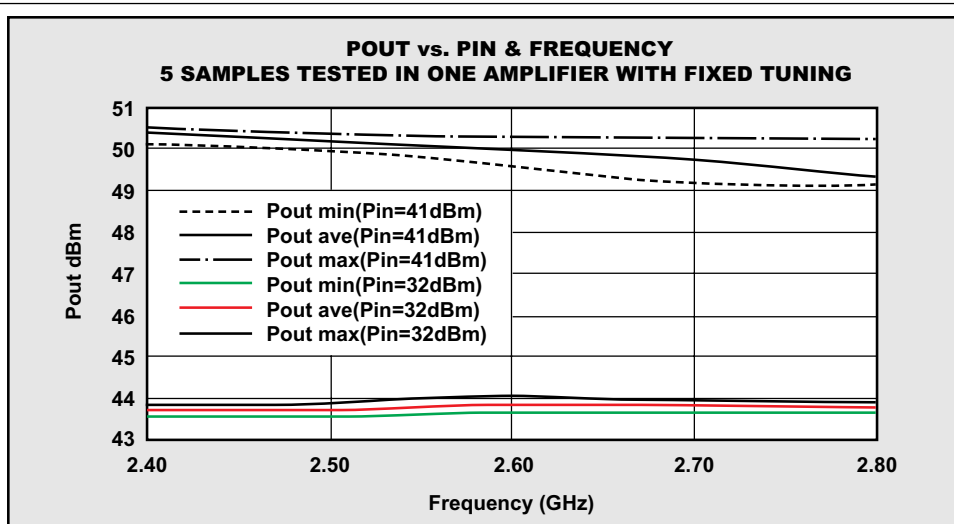
The device is used in the following conditions for the considered application: two-tone W-CDMA, Pout=40 dBm average, Ids=4.8 A, Gain=11.5 dB, η<sub>add</sub>=16%, IM3=-37 dBc, and the device flange temperature is Tf2=80°C.

**Step1-Pdiss: Calculation**

**Pdiss.2=VdsIds+Pin-Pout=**  
**12x4.8+10[(40-11.5)/10]-3]-10[(40/10)-3]=**  
**57.6+0.71-10=48.3 W**

**Step2-Calculation of Rth2 for Tf2=80°C and Pdiss.2=48.3 W**

The methodology described in the Microwave & RF October 2000 issue<sup>(2)</sup> is used with the following initial values:



**Figure 10. Device Performance Consistency**

$R_{th1} = 1.1 \text{ K/W}$  maximum and  $T_{ch1} = 25 + 1.1 \times 48 = 77.8^\circ\text{C}$ :

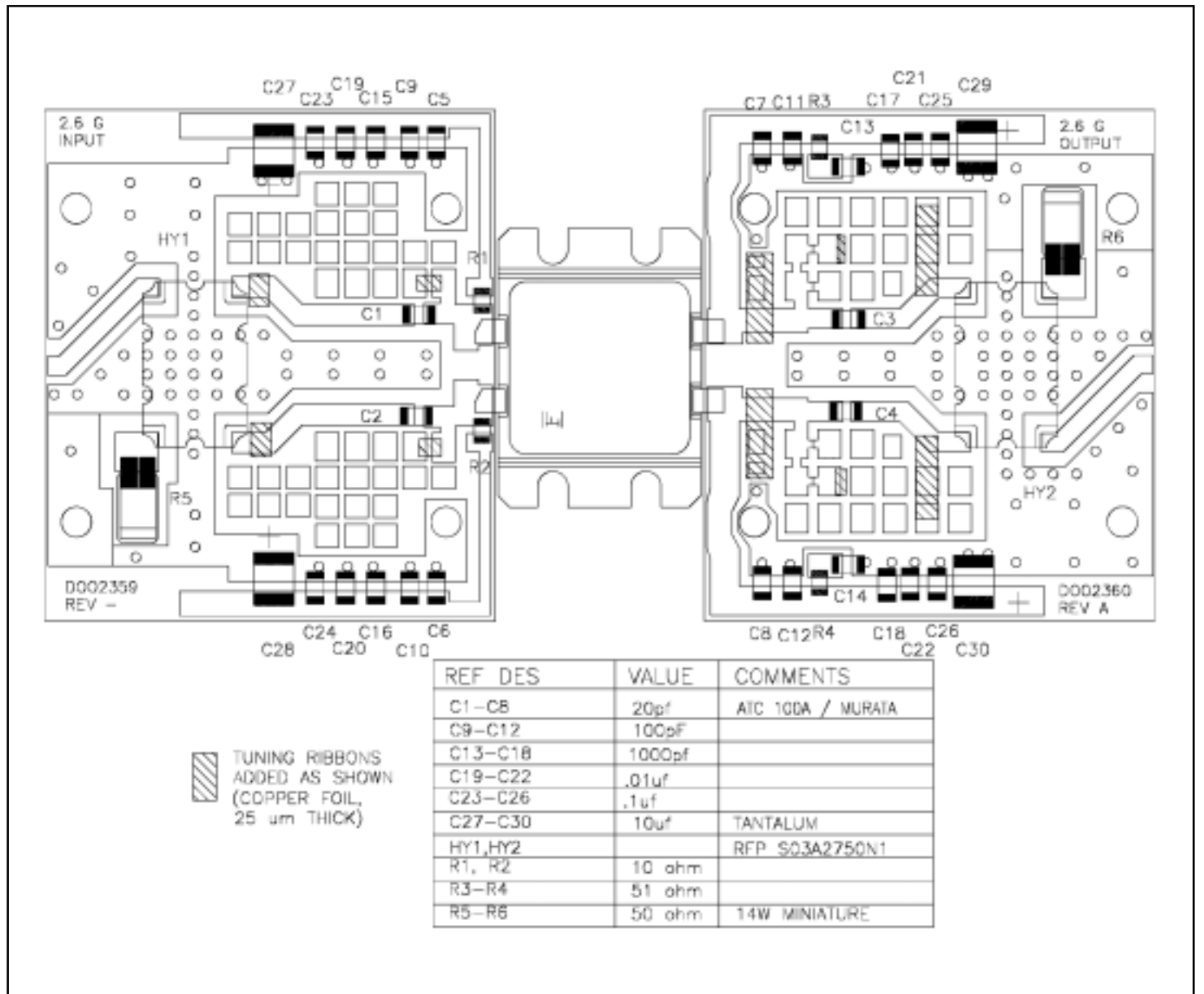
After three iterations the new  $R_{th}$  calculated value is  $R_{th2} = 1.3 \text{ k/W}$  maximum (worst case) and  $T_{ch2} = 80 + 1.3 \times 48.3 = 142.8^\circ\text{C}$ .

**Step3-Calculate MTTF**

Curve Figure 21 gives a  $MTTF = 2 \times 10^7$  hours for this temperature.

**Maximum power dissipated versus flange temperature**

It will be assumed that the maximum channel temperature is the recommended one:  $T_{ch} = 145^\circ\text{C}$ . Please note that this  $T_{ch}$  is not the absolute maximum rating  $T_{ch}$  that is  $175^\circ\text{C}$ . By using the same methodology used above, first  $R_{th}$  is calculated versus flange



**Figure 11. Amplifier Circuit with Tuning Element Positions Optimized for Two-Tone W-CDMA IM3 Performance at Pout=40dBm Average**

temperature and power dissipated and the channel temperature is limited at Tch=145°C. Table 5 shows the results of calculating Rth for various Tflange, and the resultant P<sub>DISS</sub> max for Tch=145°C.

Remark: For Tch=175°C the device MTTF will be 6x10<sup>5</sup> hours. That is a respectable value for an absolute maximum rating value.

### Measured Results

The performance obtained with the FLL810IQ-3C using the circuitry of Figure 11 is presented in the following graphs. Table 6 shows a summary of performance as original targeted specifications. This table shows that all the targeted goals were met or exceeded.

The data presented are the averaged ones across a population of four amplifiers.

For all these graphs, all four amplifiers were tuned for optimum Two-Tone W-CDMA IM3 performance at Vds=12 V, and Idsq=5 A, f=2.6 GHz, Pout=40dBm average, and not returned for the other frequencies. This demonstrates broadband performance.

The W-CDMA signal source was an HP 4433B system, Test W-CDMA (3.84Mcps, Test model 1 w/64 DPCH). ACPR was measured using a Spectrum Analyzer and 'Delta Marker Method' with a resolution bandwidth of 100 KHz and a video bandwidth of 100 Hz.

Figure 12 shows Gain vs. Frequency for each amplifier.

Figure 13 shows Pout and η<sub>add</sub> performance

versus Input Power, Pin, at 2.6 GHz.

Figure 14 shows Pout vs. Pin and Frequency.

Figure 15 shows Two-Tone CW IM3 and η<sub>add</sub> versus Pout at 2.6 GHz and Δf=5 MHz.

Figure 16 shows Two-Tone CW IM3 vs. Pin and Frequency at Δf=5 MHz.

Figure 17 shows Two-Tone W-CDMA IM3 and η<sub>add</sub> versus Pout at 2.6 GHz and Δf=10 MHz.

Figure 18 shows Two-Tone W-CDMA IM3 vs. Pout and Frequency at Δf=10 MHz.

Figure 19 shows W-CDMA ACPR at ±5MHz and η<sub>add</sub> vs. Pout at f= 2.6 GHz.

Figure 20 shows W-CDMA ACPR at ±5MHz vs. Pout and Frequency.

Figure 21 shows the MTTF versus channel temperature in °C.

### Conclusion

The FLL810IQ-3C device exhibits a better linearity at high output levels associated with a better power-added efficiency than conventional GaAs FET devices previously available. A balanced amplifier designed around this device demonstrated excellent performance. Gain was 12.0 dB, with less than 0.6 dB peak-to-peak flatness. External match was excellent, better than 13 dB return loss being

demonstrated. Linearity was shown three ways, with ACPR of <-45 dBc at 40 dBm out, and IM3 for both CW and WCDMA modulated signals being <-35 dBc for 40 dBm average power out. Class AB operation yielded high efficiency of 15%. Performance consistency was demonstrated by testing five devices in one amplifier with a fixed tuning, and tuning and testing four separate amplifiers with good results. This design can be used as a basis for MMDS power amplifier applications.

### Notes

(1). J. Shumaker, R. Basset and A. Skuratov, "High-Power GaAs FET Amplifiers: Push-Pull versus Balanced Configurations. Example W-CDMA (2.11-2.17 GHz), 150-W Amplifiers," Wireless Symposium 12-16 February 2001.

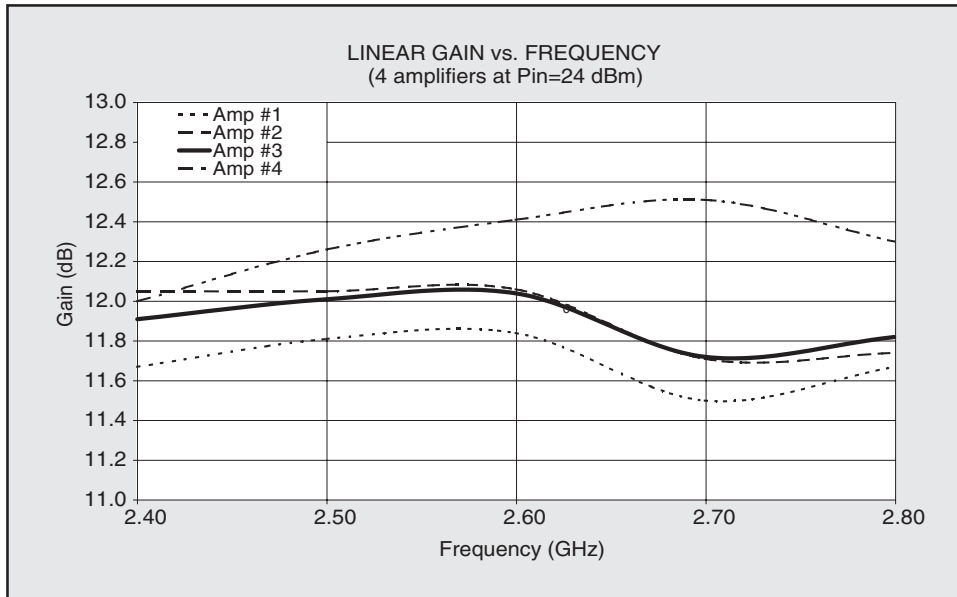
(2): R. Basset, "Understanding Thermal Basics For Microwave Power Devices", Microwave & RF, October 2000, p.101-110.

**Table 5: Maximum Power Dissipated vs. Flange Temperature**

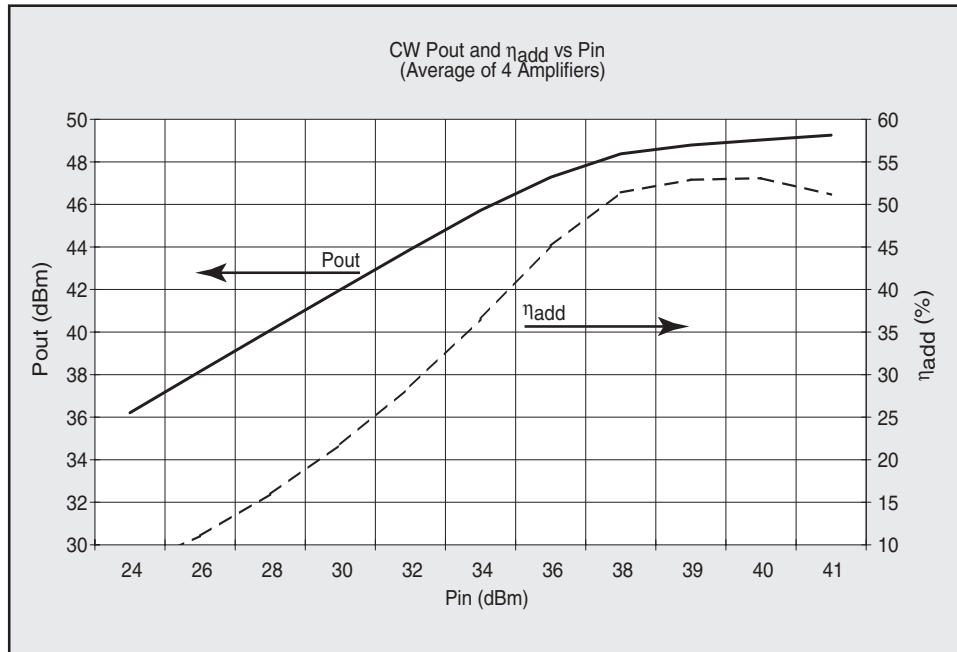
Tf in °C	Rth Max. in K/W	Tch Max. in °C	Diss. Power Max. in W	MTTF in hours
20	1.22	145	102.6	2x10 <sup>7</sup>
40	1.25	145	84.2	2x10 <sup>7</sup>
60	1.28	145	66.7	2x10 <sup>7</sup>
80	1.30	145	49.9	2x10 <sup>7</sup>
100	1.33	145	33.7	2x10 <sup>7</sup>
120	1.34	145	18.7	2x10 <sup>7</sup>
140	1.34	145	3.5	2x10 <sup>7</sup>

**Table 6: Target Specifications vs. Test Results**

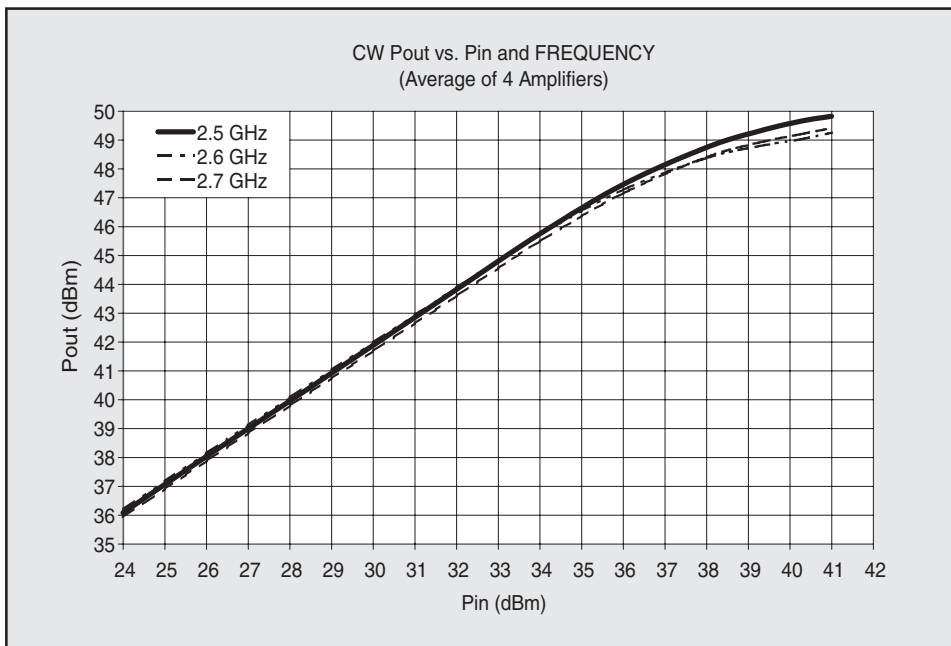
Spec	Target	Performance
Linear Gain	11.5dB	12.0dB
Gain Flatness 2.4-2.8GHz (peak-to-peak)	1.0dB	0.6dB
Saturated Output Power	49dBm	49.4dBm
Power-Added Efficiency at Psat	50%	50%
IM3 Two-Tone CW, 40dBm Pout Average	-35dBc	-36.8dBc
IM3 Two-Tone W-CDMA 40dBm Pout Average	-35dBc	-35.5dBc
ACPR at 40dBm Pout Average	-40dBc	-45dBc
η <sub>add</sub> for W-CDMA signal at 40dBm Average Pout	15%	15%



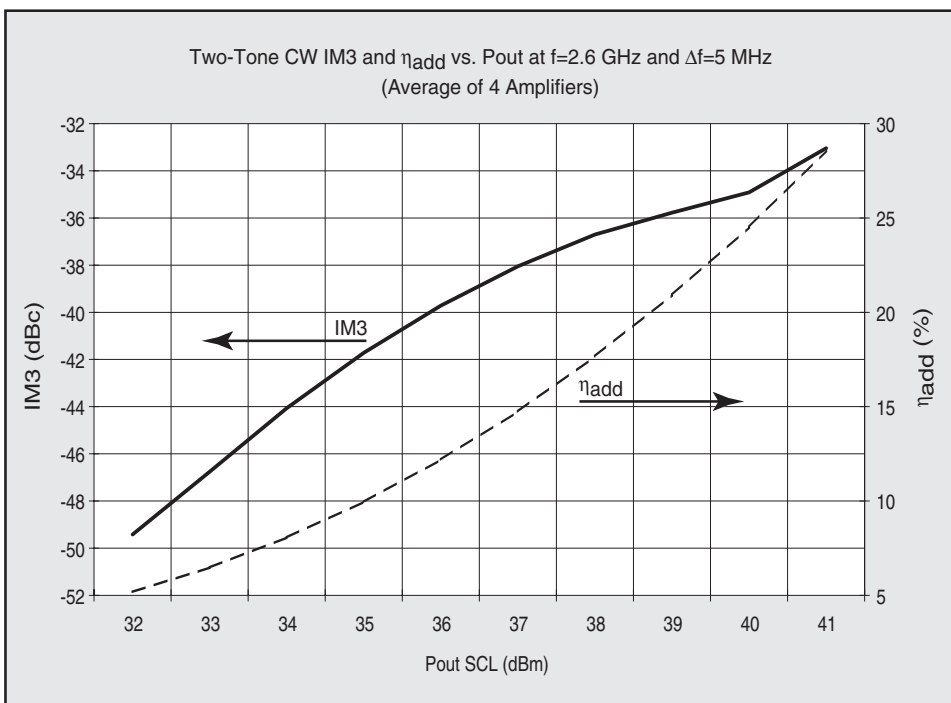
**Figure 12. CW Linear Gain vs. Frequency of 4 Amplifiers**



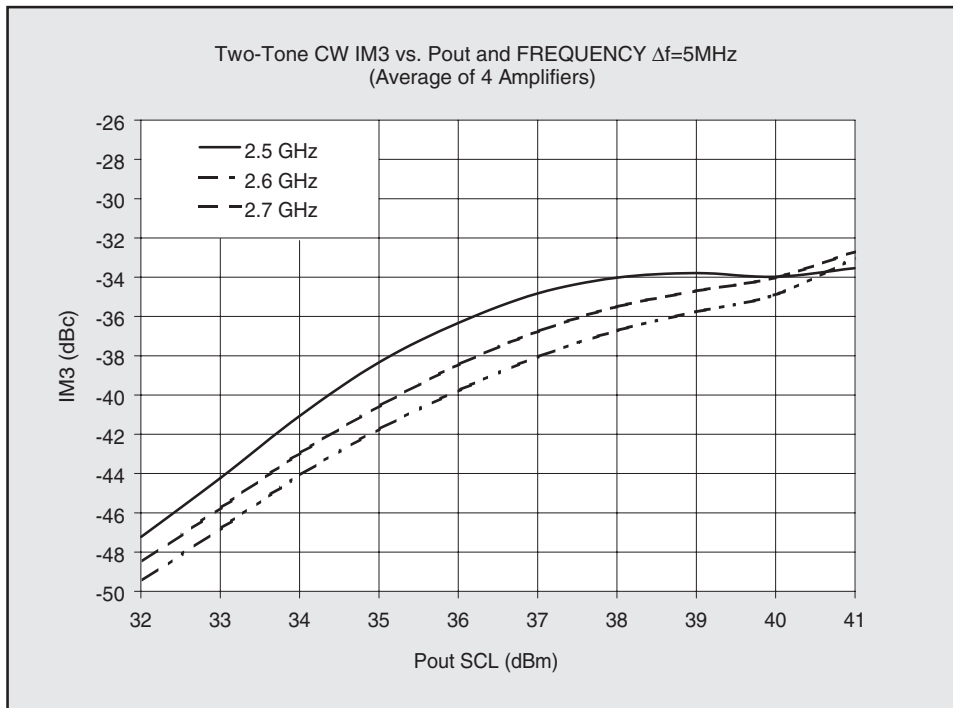
**Figure 13. CW Pout and  $\eta_{add}$  vs. Pin at f=2.6GHz**



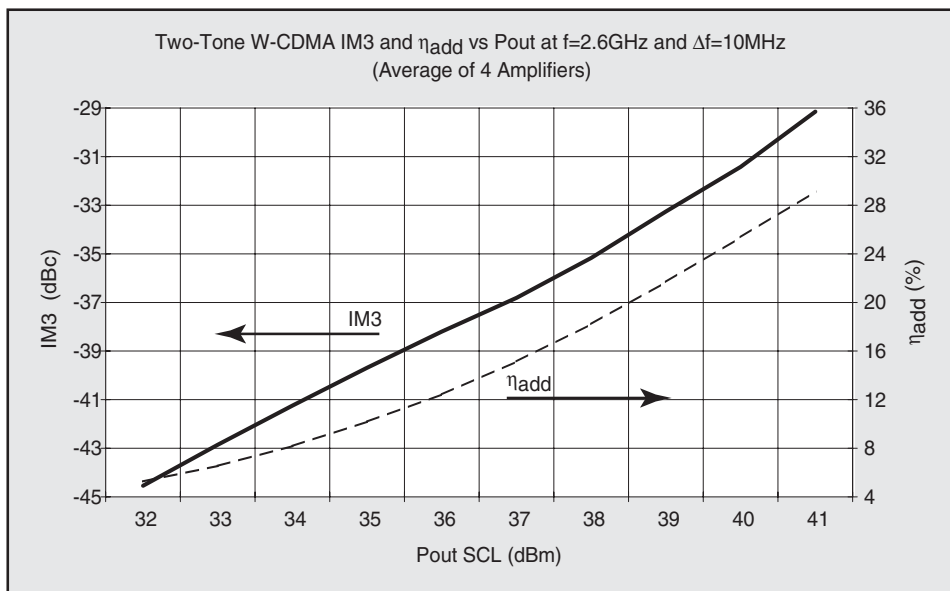
**Figure 14. CW Pout vs. Pin and Frequency**



**Figure 15. Two-Tone CW IM3 and  $\eta_{add}$  vs. Pout at  $f=2.6$ GHz and  $\Delta f=5$ MHz**



**Figure 16. Two-Tone CW IM3 vs. Pout and Frequency for  $\Delta f=5\text{MHz}$**



**Figure 17. Two-Tone W-CDMA IM3 and  $\eta_{\text{add}}$  vs. Pout at  $f=2.6\text{GHz}$  and  $\Delta f=10\text{MHz}$**

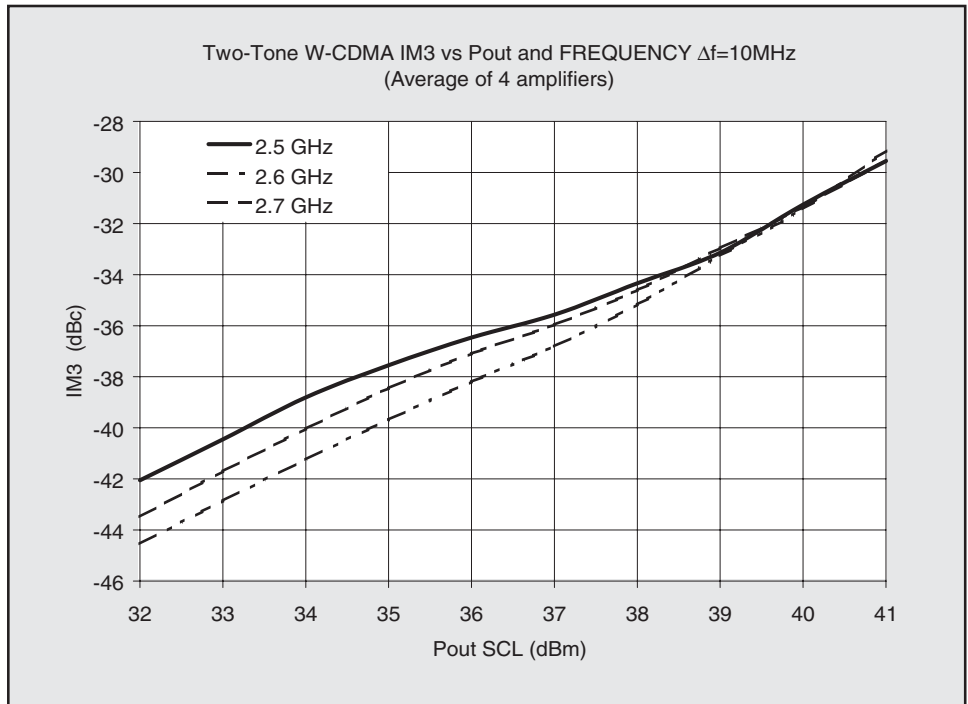


Figure 18. Two-Tone W-CDMA IM3 vs. Pout and Frequency at  $\Delta f=10\text{MHz}$

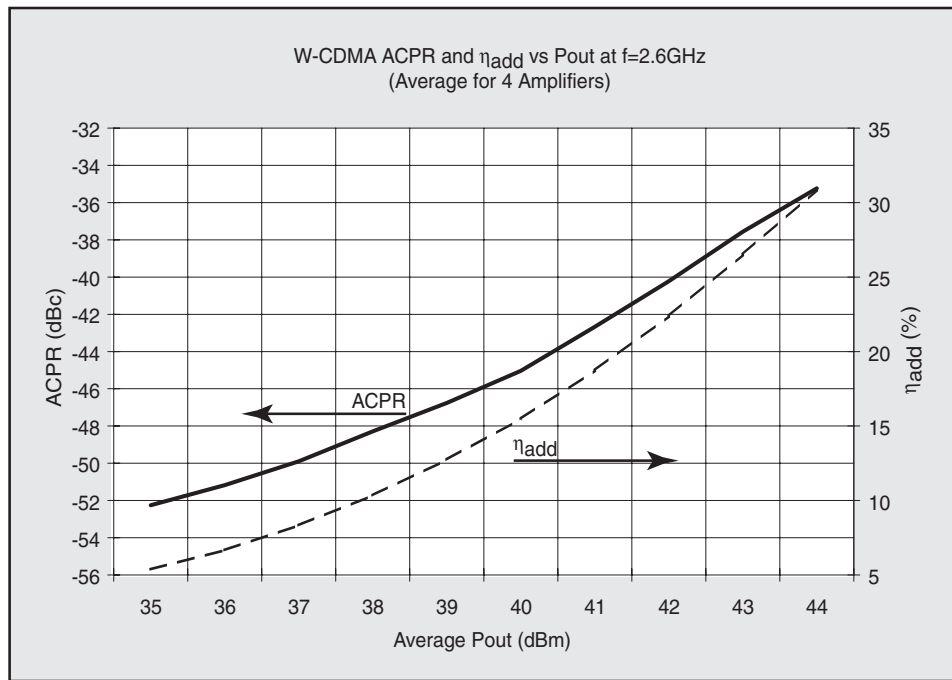
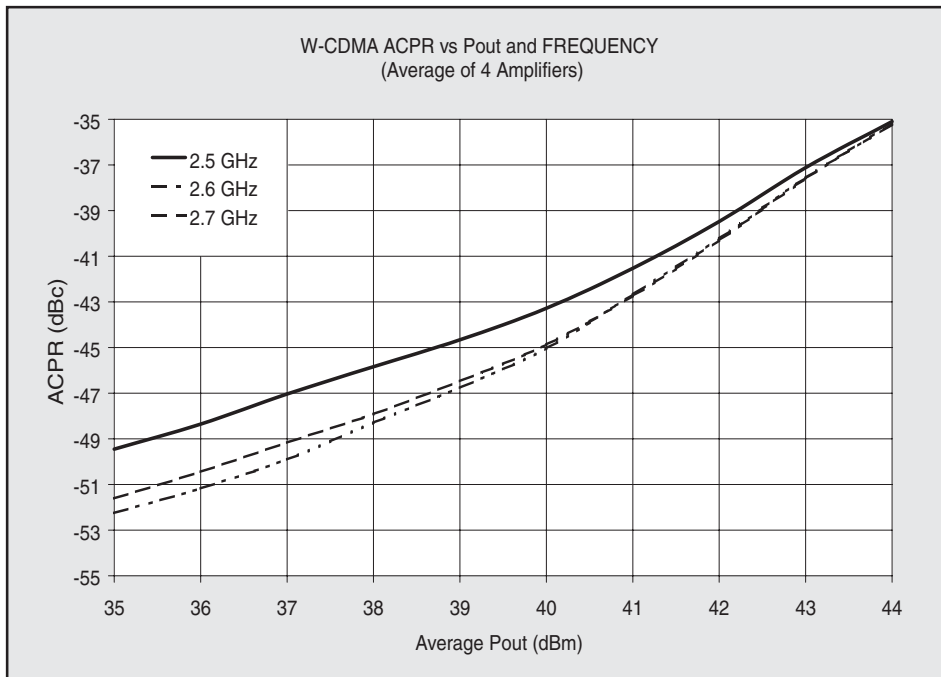
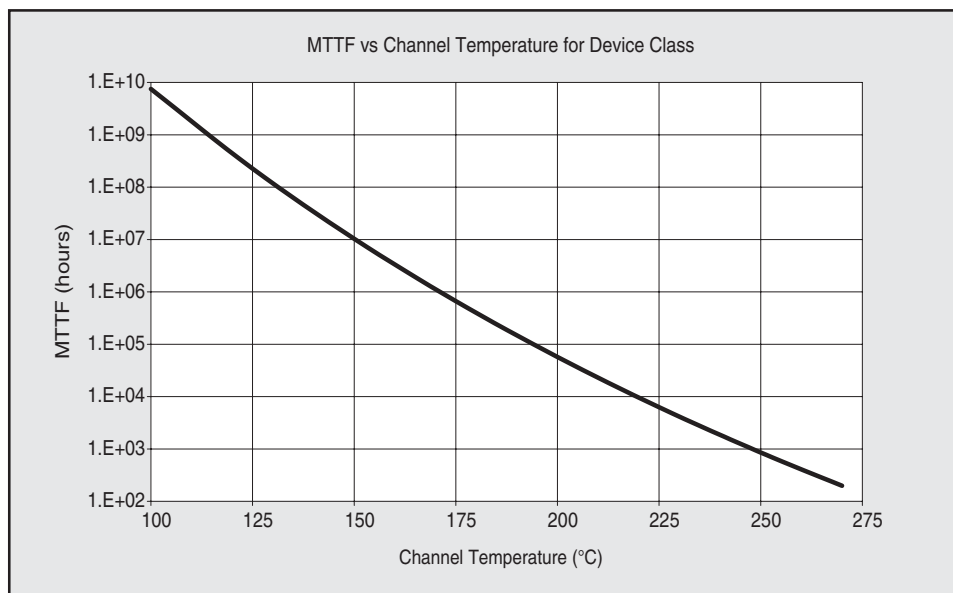


Figure 19. W-CDMA ACPR and  $\eta_{\text{add}}$  vs. Pout at  $f=2.6\text{GHz}$



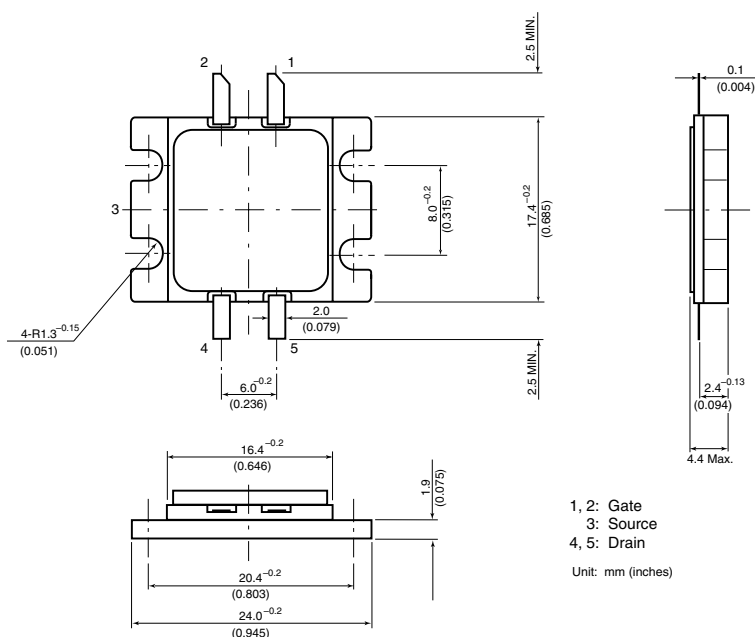
**Figure 20. W-CDMA ACPR vs. Pout and Frequency**



**Figure 21. Process MTTF vs. Channel Temperature**

# APPENDIX I - FLL810IQ-3C

## Case Style "IQ"



### ABSOLUTE MAXIMUM RATINGS (Case Temperature $T_c=25^\circ\text{C}$ )

Item	Symbol	Rating	Unit
Drain-to-Source Voltage	$V_{DS}$	15	V
Gate-to-Source Voltage	$V_{GS}$	-5	V
Total Power Dissipation	$P_T$	117	W
Storage Temperature	$T_{stg}$	-65 to +175	$^\circ\text{C}$
Channel Temperature	$T_{ch}$	+175	$^\circ\text{C}$

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-to-source operating voltage ( $V_{DS}$ ) should not exceed 12 volts.
2. The total gate current,  $I_{GS}$ , should be  $-52 < I_{GS} < 176\text{mA}$  with a gate resistance of  $10\Omega$  each side.

### ELECTRICAL AND THERMAL CHARACTERISTICS (Case Temperature $T_c=25^\circ\text{C}$ )

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Pinch-Off Voltage	$V_p$	$V_{DS} = 5\text{V}$ , $I_{DS} = 220\text{mA}$	-0.5	-0.3	-0.1	V
Gate-to-Source Breakdown Voltage	$V_{GSO}$	$I_{GS} = -2.2\text{mA}$	-	-	-5	V
Output Power	$P_{out}$	$V_{DS} = 12\text{V}$ $f = 2.6\text{GHz}$	48.0	49.0	-	dBm
Power-Added Efficiency	$\eta_{add}$	$I_{DS} = 5.0\text{A}$ $P_{in} = 40.0\text{dBm}$	-	50	-	%
Linear Gain	GL		11.0	12.0	-	dB
Thermal Resistance, Channel-to-Flange	$R_{th}$	12V, 4A	-	0.8	1.1	$^\circ\text{C/W}$

CASE STYLE: IQ

## APPENDIX II - Impedance Parameter Files

These are the impedance 1-port files for matching created from table 2 impedances. Listing is in Touchstone format.

**The impedance parameter file for the input Zin:**

"FLL810IQ3C\_Zin.S1P"

! Zin normalized for Device: FLL810IQ-3C  
 ! Bias: VDS = 12.0V, IDSQ = 2.5A (One Half of Push-Pull Device)  
 ! Frequency: 2.3 GHz - 2.8 GHz  
 ! Lot #: Engineering Sample Ser#:14  
 # GHz Z RI R 50

! Half FLL810IQ-3C Zin Tuned For Maximum Gain & Zouttuned for Psat  
 ! Freq (GHz) Zin real(Ohm) Z i n imaginary (Oh)  
 2.3 0.956 +0.208  
 2.4 0.532 -0.106  
 2.5 0.368 -0.118  
 2.6 0.286 +0.034  
 2.7 0.210 +0.194  
 2.8 0.170 +0.338

**The impedance parameter file for the output Zout:**

"FLL810IQ3C\_Zout.S1P"  
 ! Zout normalized for Device: FLL810IQ-3C

! Bias: VDS = 12.0V, IDSQ = 2.5A (One Half of Push-Pull Device)  
 ! Frequency: 2.3 GHz - 2.8 GHz  
 ! Lot #: Engineering Sample Ser#:14  
 # GHz Z RI R 50  
 ! Half FLL810IQ-3C Zin & Zout Tuned For Maximum Gain and Psat  
 ! Freq (GHz) Zout real (Ohm) Zout imaginary (Ohm)  
 2.3 0.272 +0.204  
 2.4 0.326 +0.118  
 2.5 0.424 -0.108  
 2.6 0.314 -0.176  
 2.7 0.196 -0.100  
 2.8 0.138 -0.064

**Linear S-Parameter file for the device:**

! FLL810IQ-3C  
 ! S-PARAMETERS  
 ! VDS = 12V, IDSQ = 2.5A  
 ! 1.5 to 3.5GHz

! Note: This S-Parameter data shows measurements performed on a single-ended push-pull FET.  
 # MHz S MA R 50

! Freq	magS11	angS11	magS21	angS21	magS12	angS1	magS22	angS22
1500	.856	137.9	1.167	39.2	.021	43.0	.841	167.3
1600	.786	131.5	1.430	25.6	.026	31.2	.805	167.9
1700	.698	124.7	1.722	10.3	.029	15.8	.790	169.2
1800	.579	118.4	2.020	-8.0	.034	0.9	.777	170.2
1900	.455	115.3	2.323	-27.7	.036	-16.4	.795	171.0
2000	.347	115.2	2.564	-48.5	.039	-39.5	.818	169.7
2100	.247	119.8	2.784	-67.9	.041	-59.6	.819	167.1
2200	.141	142.0	3.064	-90.1	.041	-84.9	.781	163.5
2300	.200	-160.2	3.418	-114.9	.039	-114.5	.668	162.4
2400	.425	-159.8	3.446	-143.7	.035	-150.5	.560	170.4
2500	.634	-179.2	3.332	-173.7	.029	170.0	.556	-175.3
2600	.738	156.5	2.845	161.4	.024	122.6	.659	-168.5
2700	.750	129.4	2.436	134.5	.023	84.7	.747	-168.5
2800	.693	94.5	2.125	113.9	.020	47.3	.822	-170.0
2900	.620	48.8	1.618	89.3	.020	12.3	.879	-172.2
3000	.601	0.2	1.345	67.3	.019	-15.0	.910	-175.1
3100	.713	-39.5	1.031	50.9	.017	-35.8	.931	-177.6
3200	.804	-68.6	.748	31.0	.014	-60.2	.922	-179.8
3300	.863	-89.7	.587	19.4	.015	-70.4	.936	178.2
3400	.895	-104.3	.420	9.2	.014	-85.8	.936	176.2
3500	.909	-115.6	.335	0.5	.009	-96.7	.951	174.2