

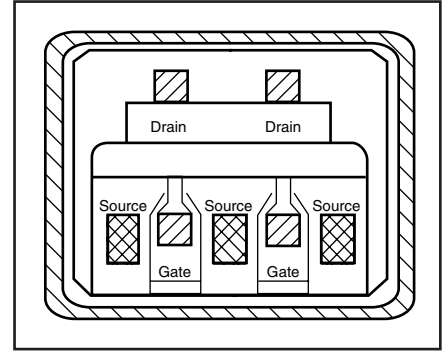
FEATURES

- High Output Power: $P_{1dB} = 27.0\text{dBm(Typ.)}$
- High Gain: $G_{1dB} = 7.0\text{dB(Typ.)}$
- High PAE: $\eta_{add} = 32\%\text{(Typ.)}$
- Proven Reliability

DESCRIPTION

The FLK057XV chip is a power GaAs FET that is designed for general purpose applications in the Ku-Band frequency range as it provides superior power, gain, and efficiency.

Eudyna stringent Quality Assurance Program assures the highest reliability and consistent performance.



ABSOLUTE MAXIMUM RATING (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_{tot}	$T_c = 25^\circ\text{C}$	3.75	W
Storage Temperature	T_{stg}		-65 to +175	$^\circ\text{C}$
Channel Temperature	T_{ch}		175	$^\circ\text{C}$

Eudyna recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 4.4 and -0.2 mA respectively with gate resistance of 1000 Ω .
3. The operating channel temperature (T_{ch}) should not exceed 145 $^\circ\text{C}$.

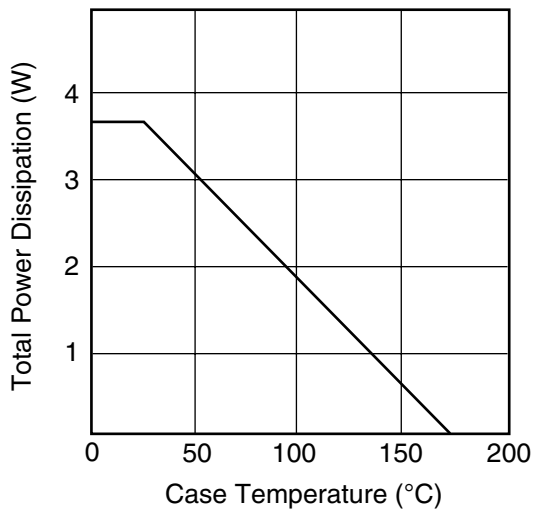
ELECTRICAL CHARACTERISTICS (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	I_{DSS}	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}$	-	200	300	mA
Transconductance	g_m	$V_{DS} = 5\text{V}, I_{DS} = 125\text{mA}$	-	100	-	mS
Pinch-off Voltage	V_p	$V_{DS} = 5\text{V}, I_{DS} = 10\text{mA}$	-1.0	-2.0	-3.5	V
Gate Source Breakdown Voltage	V_{GSO}	$I_{GS} = -10\mu\text{A}$	-5	-	-	V
Output Power at 1dB Gain Compression Point	P_{1dB}	$V_{DS} = 10\text{V}$ $I_{DS} \approx 0.6I_{DSS}$ $f = 14.5\text{GHz}$	26	27	-	dBm
Power Gain at 1dB Gain Compression Point	G_{1dB}		6	7	-	dB
Power-added Efficiency	η_{add}		-	32	-	%
Thermal Resistance	R_{th}	Channel to Case	-	20	40	$^\circ\text{C/W}$

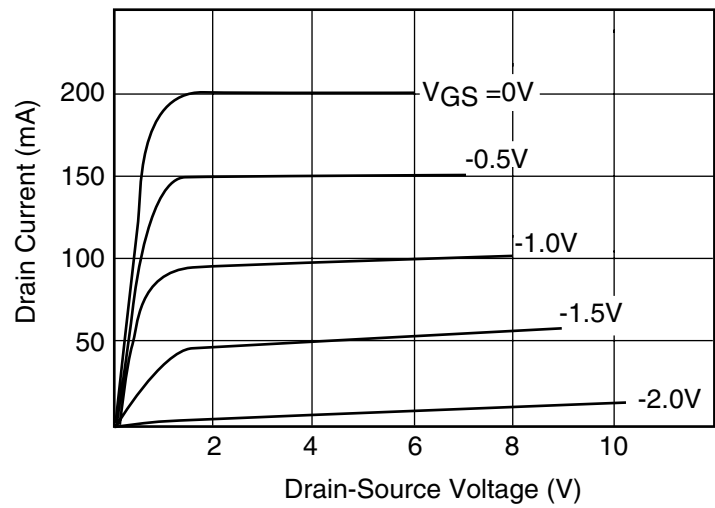
Note: RF parameter sample size 10pcs. criteria (accept/reject)=(2/3)

The chip must be enclosed in a hermetically sealed environment for optimum performance and reliability.

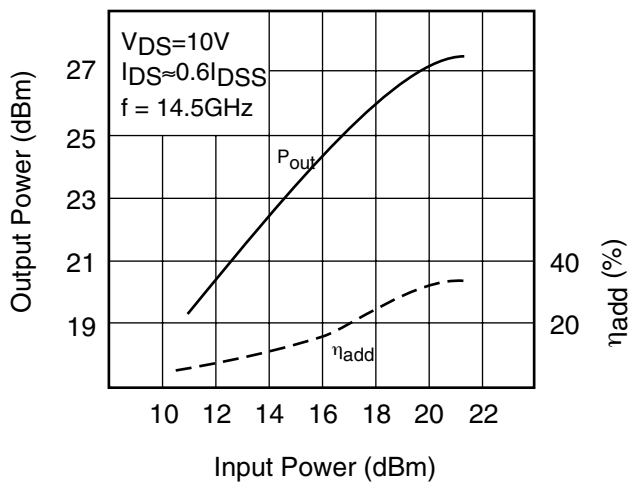
POWER DERATING CURVE



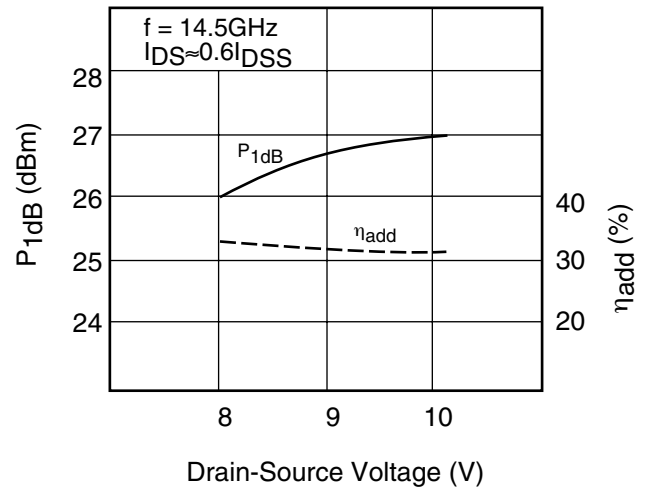
DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE



OUTPUT POWER vs. INPUT POWER



P_{1dB} & η_{add} vs. V_{DS}



S-PARAMETERS

$V_{DS} = 10V$, $I_{DS} = 120mA$

FREQUENCY (MHZ)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	1.000	-6.4	6.959	175.9	.004	86.4	.500	-3.0
500	.989	-31.3	6.696	159.7	.020	72.5	.488	-14.6
1000	.965	-58.9	6.033	141.7	.036	57.1	.460	-27.4
1500	.940	-81.4	5.262	126.6	.046	44.7	.430	-37.7
2000	.919	-99.1	4.551	114.2	.054	35.1	.406	-46.1
2500	.904	-113.1	3.952	103.9	.058	27.4	.389	-53.2
3000	.893	-124.1	3.462	95.1	.061	21.2	.380	-59.3
3500	.885	-133.2	3.062	87.2	.063	16.1	.376	-65.0
4000	.879	-140.7	2.735	80.2	.065	11.7	.377	-70.2
4500	.875	-147.0	2.464	73.7	.065	7.9	.380	-75.2
5000	.872	-152.5	2.236	67.7	.066	4.5	.386	-79.9
5500	.870	-157.4	2.043	62.0	.066	1.5	.394	-84.5
6000	.869	-161.7	1.877	56.6	.067	-1.4	.404	-88.9
6500	.868	-165.6	1.733	51.4	.067	-4.0	.414	-93.1
7000	.867	-169.1	1.607	46.4	.067	-6.4	.426	-97.3
7500	.867	-172.4	1.496	41.5	.067	-8.8	.438	-101.3
8000	.867	-175.4	1.398	36.8	.067	-11.0	.451	-105.1
8500	.867	-178.3	1.309	32.1	.066	-13.1	.464	-108.9
9000	.867	179.0	1.230	27.6	.066	-15.1	.477	-112.6
9500	.867	176.5	1.158	23.2	.066	-17.1	.490	-116.1
10000	.868	174.1	1.092	18.9	.066	-19.0	.504	-119.6
10500	.868	171.8	1.032	14.6	.065	-20.8	.517	-123.0
11000	.869	169.6	.977	10.5	.065	-22.6	.531	-126.3
11500	.870	167.5	.927	6.4	.064	-24.4	.544	-129.5
12000	.870	165.4	.880	2.3	.064	-26.1	.557	-132.7
12500	.871	163.4	.836	-1.7	.064	-27.8	.570	-135.8
13000	.872	161.5	.795	-5.6	.063	-29.4	.583	-138.8
13500	.873	159.6	.758	-9.4	.063	-31.0	.596	-141.8
14000	.874	157.8	.722	-13.2	.062	-32.6	.609	-144.7
14500	.875	156.1	.689	-16.9	.061	-34.1	.621	-147.6
15000	.876	154.3	.657	-20.6	.061	-35.6	.633	-150.3
15500	.877	152.6	.628	-24.2	.060	-37.1	.645	-153.1
16000	.879	151.0	.600	-27.8	.060	-38.6	.656	-155.8
16500	.880	149.4	.574	-31.3	.059	-40.0	.667	-158.4
17000	.881	147.8	.549	-34.8	.059	-41.5	.678	-161.0
17500	.882	146.3	.525	-38.2	.058	-42.9	.689	-163.5
18000	.883	144.7	.503	-41.5	.057	-44.2	.699	-166.0
18500	.885	143.2	.482	-44.8	.057	-45.6	.709	-168.4
19000	.886	141.8	.462	-48.1	.056	-46.9	.719	-170.8
19500	.887	140.3	.442	-51.3	.055	-48.2	.728	-173.2
20000	.888	138.9	.424	-54.4	.055	-49.5	.737	-175.5

NOTE:* The data includes bonding wires.

n: number of wires Gate n=2 (0.2mm length, 25µm Dia Au wire)
 Drain n=2 (0.2mm length, 25µm Dia Au wire)

CHIP OUTLINE

