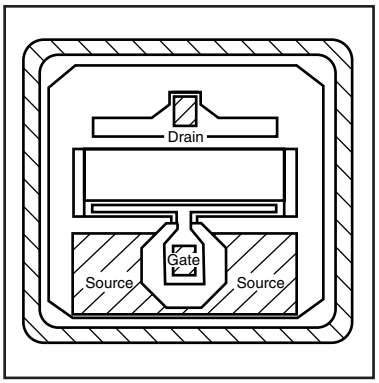
FLC087XP

GaAs FET & HEMT Chips

FEATURES

- High Output Power: P_{1dB} = 28.5dBm(Typ.)
- High Gain: G_{1dB} = 7.0dB(Typ.)
- High PAE: η_{add} = 31.5%(Typ.)
- Proven Reliability



DESCRIPTION

The FLC087XP chip is a power GaAs FET that is designed for general purpose applications in the C-Band frequency range as it provides superior power, gain, and efficiency.

Eudyna stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING (Ambient Temperature Ta=25°C)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_{tot}	T_c = 25°C	4.16	W
Storage Temperature	T_{stg}		-65 to +175	°C
Channel Temperature	T_{ch}		175	°C

Eudyna recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 4.8 and -0.5 mA respectively with gate resistance of 400Ω.
3. The operating channel temperature (T_{ch}) should not exceed 145°C.

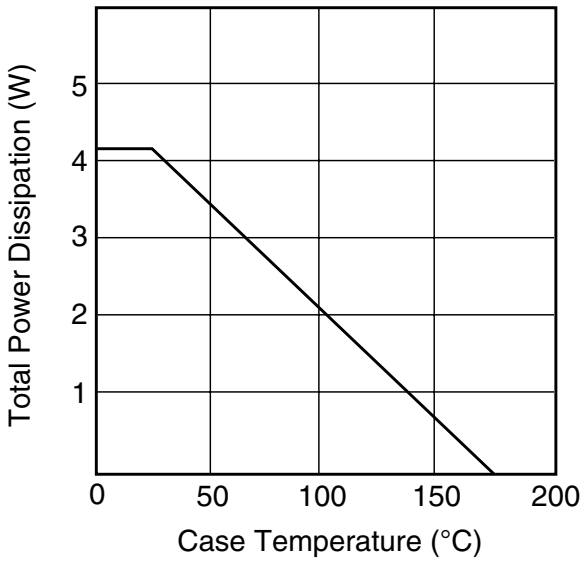
ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0V	-	300	450	mA
Transconductance	g_m	V_{DS} = 5V, I_{DS} = 200mA	75	150	-	mS
Pinch-off Voltage	V_p	V_{DS} = 5V, I_{DS} = 15mA	-1.0	-2.0	-3.5	V
Gate Source Breakdown Voltage	V_{GSO}	I_{GS} = -15μA	-5	-	-	V
Output Power at 1dB Gain Compression Point	P_{1dB}	V_{DS} = 10V $I_{DS} \approx 0.6I_{DSS}$ f = 8GHz	27.5	28.5	-	dBm
Power Gain at 1dB Gain Compression Point	G_{1dB}		6.0	7.0	-	dB
Power-added Efficiency	η_{add}		-	31.5	-	%
Thermal Resistance	R_{th}	Channel to Case	-	25	36	°C/W

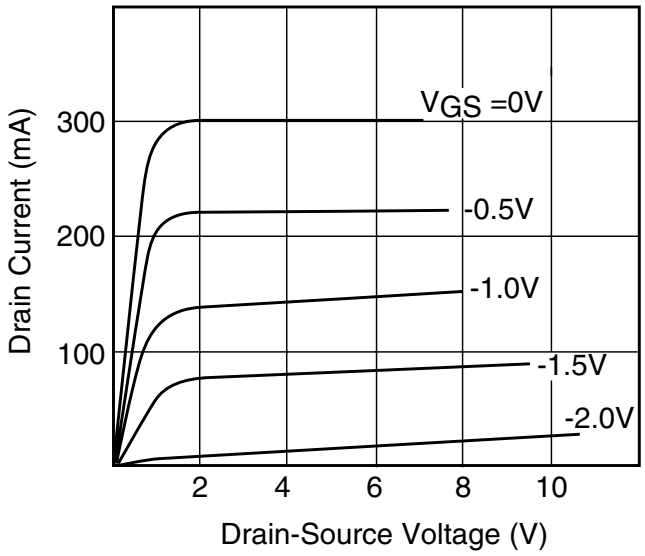
Note: RF parameter sample size 10pcs. criteria (accept/reject)=(2/3)

The chip must be enclosed in a hermetically sealed environment for optimum performance and reliability.

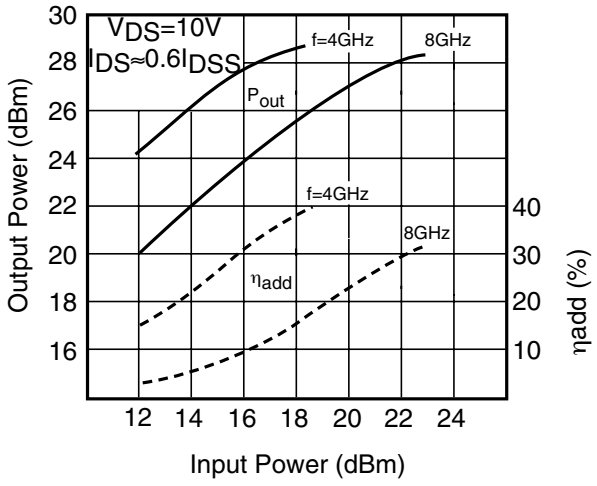
POWER DERATING CURVE



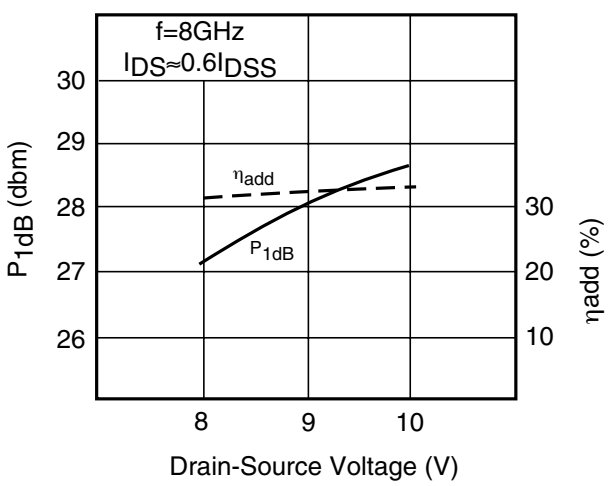
DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE



OUTPUT POWER vs. INPUT POWER



P_{1dB} & η_{add} vs. V_{DS}



S-PARAMETERS

V_{DS} = 10V, I_{DS} = 200mA

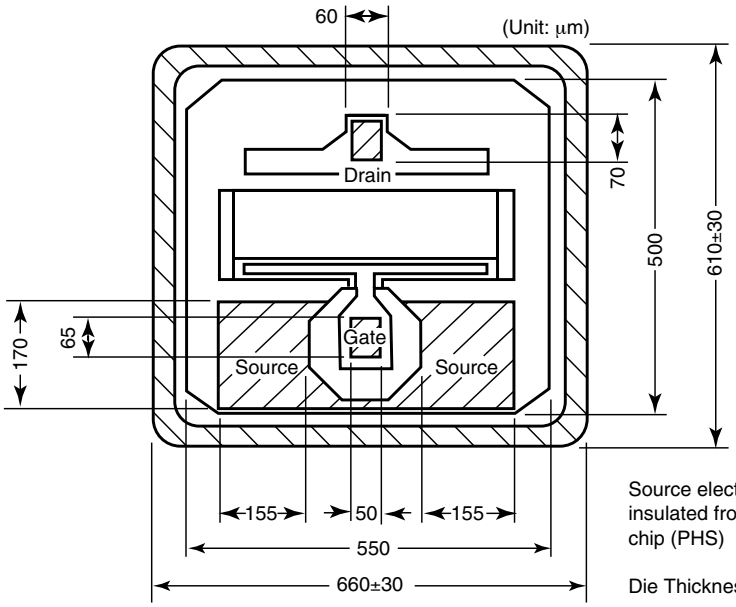
FREQUENCY	S11		S21		S12		S22	
(MHZ)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	.998	-11.7	9.704	172.7	.006	83.8	.510	-4.7
500	.965	-54.6	8.567	145.8	.026	61.3	.467	-21.1
1000	.914	-92.8	6.593	121.3	.039	42.4	.399	-34.2
1500	.883	-116.8	5.088	104.7	.046	31.3	.355	-42.2
2000	.866	-132.5	4.067	92.4	.048	24.5	.332	-48.2
2500	.857	-143.5	3.363	82.4	.050	20.0	.323	-53.7
3000	.852	-151.7	2.856	73.7	.051	16.9	.320	-59.0
3500	.848	-158.1	2.478	65.9	.051	14.6	.323	-64.3
4000	.846	-163.4	2.186	58.6	.052	12.9	.330	-69.7
4500	.845	-167.9	1.954	51.8	.052	11.5	.338	-74.9
5000	.845	-171.8	1.765	45.2	.052	10.5	.349	-80.2
5500	.845	-175.3	1.608	38.9	.052	9.6	.362	-85.3
6000	.845	-178.4	1.476	32.7	.053	8.9	.375	-90.4
6500	.845	178.7	1.362	26.7	.053	8.4	.390	-95.3
7000	.846	176.1	1.264	20.8	.053	8.0	.406	-100.2
7500	.847	173.6	1.177	15.0	.053	7.6	.422	-105.0
8000	.847	171.2	1.099	9.3	.053	7.3	.439	-109.6
8500	.848	169.0	1.030	3.7	.053	7.1	.456	-114.2
9000	.849	166.8	.967	-1.9	.053	7.0	.474	-118.7
9500	.850	164.7	.909	-7.4	.053	6.9	.492	-123.1
10000	.852	162.7	.856	-12.8	.054	6.8	.511	-127.5
10500	.853	160.8	.806	-18.1	.054	6.7	.529	-131.7
11000	.854	158.9	.760	-23.4	.054	6.7	.548	-135.9
11500	.855	157.1	.716	-28.7	.054	6.7	.567	-140.0
12000	.857	155.3	.675	-33.9	.055	6.6	.585	-144.0

NOTE:* The data includes bonding wires.

n: number of wires
Gate n=1 (0.3mm length, 25μm Dia Au wire)
Drain n=1 (0.3mm length, 25μm Dia Au wire)
Source n=4 (0.3mm length, 25μm Dia Au wire)

Download S-Parameters, click here

CHIP OUTLINE



Source electrodes are electrically insulated from the bottom of the chip (PHS)

Die Thickness: 60±20μm