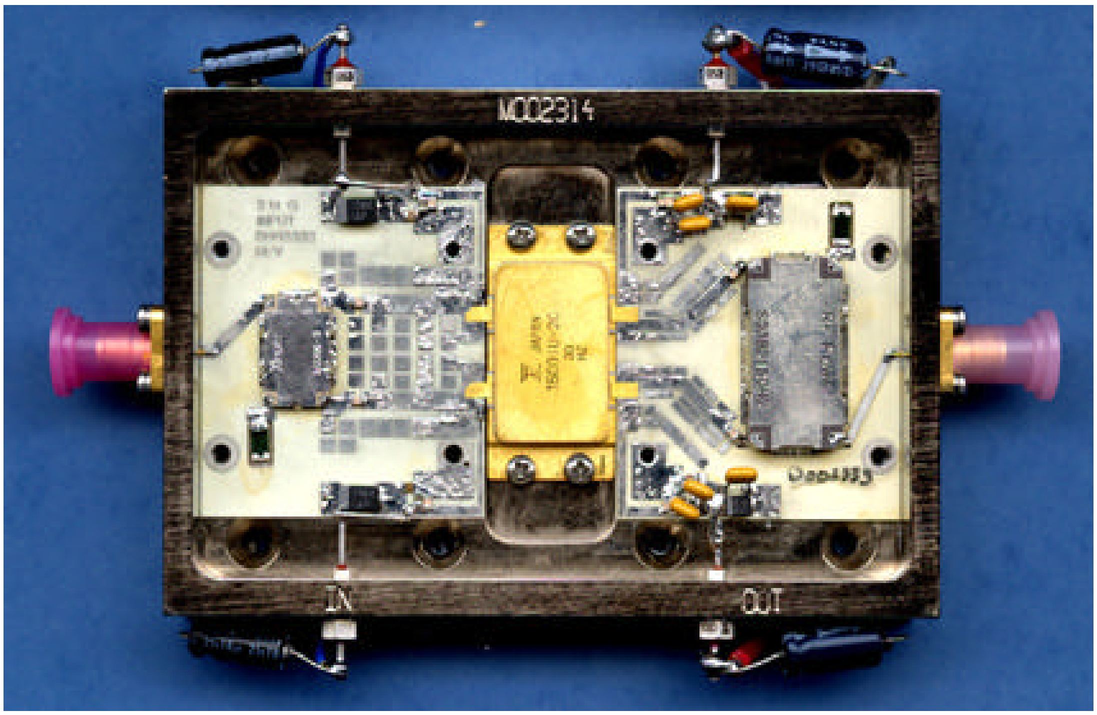
FUJITSU APPLICATION NOTE - No 008

150-W, 2.11- 2.17 GHz Balanced Compact Amplifier For IMT-2000 Base-Station Application Using The FLL1500IU-2C GaAs FET Device



FEATURES

- **Targeted WCDMA ACPR at 20W average Pout**
- **Over 150 Watts P_{out} over entire band**
- **High gain**
- **Good repeatability**
- **Easy tuning for Power, WCDMA ACPR, and IMD**
- **High MTTF > 10^6 hours @ T_{CH} =175 °C**
- **High linearity**
- **High Power-Added Efficiency**

SUMMARY: A 150-W balanced compact amplifier design using Er=3.48 dielectric material for the 2.11-2.17 GHz WCDMA band using the Fujitsu FLL1500IU-2C GaAs FET device is presented. Full circuit design details as well as the measured results for class A-B operation are provided.

FUJITSU

Circuit Description

The circuitry described in this application note provides the RF engineer with a design for a 150-W balanced amplifier. This design is suited for WCDMA applications requiring high linearity and efficiency. The high linearity is obtained with a minimum of tuning components and this amplifier can operate over the entire 2.11-2.17 GHz WCDMA band. This amplifier exhibits a WCDMA ACPR performance of -41 dBc typical at 20 W (43 dBm) output power. The aim was to realize this design in a minimum footprint, using an inexpensive circuit board material.

Balanced vs. Push-Pull Configuration Approach

Both balanced and push-pull configurations(1) result in a similar basic performance when operated in any class of operation and in bandwidth smaller than one octave. Both can be designed for similar linearity and efficiency performance as an amplifier for commercial application with relatively narrow bandwidth (10%). However the balanced approach has the following advantages in system use.

- Better stability
- Better external match
- Good isolation between the two identical sides of the device
- Ease to design quadrature couplers and to integrate them to the amplifier layout

The example presented herein will be that of the balanced circuit.

150-W WCDMA Amplifier Components

The RF circuit elements of the 150-W amplifier are the Fujitsu FLL1500IU-2C, 150-W power GaAs FET, two surface-mount 90-degree hybrid couplers, several capacitors and resistors mounted on a dielectric substrate. A detailed part list can be found in Figure 8.

FLL1500IU-2C Device Description

The FLL1500IU-2C utilizes two pairs of 40 W Au gate power GaAs FET chips that are mounted within the Fujitsu IU package. This package has two Gate and two Drain connections. The four chips are matched for DC and RF performance. Impedance matching networks are used within the package to raise the input and output impedances to allow for easier external circuit board tuning. The 0.6µm Au gate FET chip has an MTTF of 1×10^{8} hours for a channel temperature of 150°C, at the overvoltage condition of 15V drain-to-source. For those who need to calculate reliability at other temperatures, the activation energy for this transistor type has been measured at Ea=1.79 eV, and the life extrapolated from measured data. See Figure 13 at the end of the data section. The transistor chips and the IU package have been optimized for low thermal resistance, typically 0.55 K/W. Additionally, the IU package is hermetically sealed for applications where extreme environmental conditions may be encountered.

Quadrature Couplers and Board Material Description

The 2.11–2.17 GHz, 150-W linear amplifier design presented in the following sections is achieved by using surface-mount 90-degree couplers and inexpensive Rogers 4350 moderate dielectric constant (ε_r) substrate. All components used in the design are commercially available. Surface-mount couplers were used which gives some size reduction at these frequencies over creating a printed coupler design. The substrate's physical and electrical parameters are summarized below.

ε_r	h (mm)	Metallization	Metal Thickness (mm)
3.48	.787	Cu	.034

Table 1. Rogers 4350 substrate parameters

DC Bias Circuit Topology

Gate Biasing Circuit

The gate biasing circuit has several functions:

- To maintain a constant gate-to-source voltage.
- To be able to supply a negative and positive gate current.
- To protect the gate by limiting the gate current when the device goes in breakdown (drain-to-gate or gate-to-source) or when the gate-to-source junction is biased with a positive voltage. These abnormal operating conditions for the devices can be due to an operator error, an overdrive, a system problem or ESD.
- To stabilize the device in case a negative resistance appears in the gate at any frequency where the device has gain.
- To filter the signal and the products generated by the device input from very low frequencies to high frequencies without affecting the device input matching circuit.
- Isolate the gate from any signal coming from the drain through the biasing connections, to minimize the coupling gate-to-drain (feedback) at any frequency where the device has a gain.

Figure 1A shows the generic amplifier gate biasing circuit, and figure 2 shows the circuit in more detail. Starting from the input matching circuit, it consists of a gate resistor, Rg, connected to the input of a quarter-wave length high impedance microstrip line short-circuited at its extremity by a several capacitors. The impedance of the biasing circuit connected in parallel to the input matching circuit is very high since it is a resistor in series with a quarter-wave short-circuited high impedance microstrip line. Thus the resistor and bypass have no effect on the input matching circuit.
Several capacitors are connected at the extremity of the quarter-wave length line. The complete case starts with a small value, few pF, to realize a good RF short circuit in the amplifier RF passband, then 100 pF, 1, 10, 100 nF, 1 and 10 uF to realize a good filtering (short circuit to the ground) from very low frequencies up to the fundamental frequency. Capacitors with low parasitic series inductance and resistor should be used. Not all values are required for every application.

Since the average current in the gate, Igs, is relatively low (absolute value is less than 50 mA), the current handling of the gate bias circuit doesn't have to be higher than 100 mA. It means a high impedance transmission line can be used.
The value of the gate resistance is a compromise between minimum and maximum limits.

Minimum Resistance Limit

- Low Frequency Stabilization: The bias resistor should be connected as close as possible to the gate. For relatively low frequencies, the DC blocking capacitors (picofarads) are open circuits, the decoupling capacitors (microfarads) are short circuits and the quarter-wave lines at RF frequencies become short lines. It means for low frequencies, the gates are connected to the ground through the gate resistors. If a negative resistance (R<0) appears in the gates and the sum of the resistors (R+Rg>0) is positive the device will be stable. This function requires Rg to have a sufficient value and the connection to the ground to be short for low frequencies. Connecting the resistor close to the gate reduces the connection length to the ground.
- The gate current limitation under breakdown, large drive and EDS requires a sufficient Rg value but this value for the below reasons has to be limited.

Maximum Resistance Limit

- The gate voltage, Vgs, should be maintained constant versus the drive level i.e. versus Igs. . The gate current, Igs, versus drive can change from –2 to 70 mA total. If the desired Vgs maximum variation versus drive is about 200 mV, the maximum value of Rg is RgMax=200/70=3 ohms total It means 6 ohm resistor maximum for each side of the device.

The device thermal runaway limits also the maximum value of Rg. The runaway mechanism can be explained as follows. Vgs=Vgg-Igs*Rg, with Igs negative without RF drive. Thus when the temperature increases, Igs becomes more negative and Vgs increases. This increase of Vgs increases Ids, which increases the power dissipated in the device i.e. the channel temperature. The channel temperature rise makes Igs more negative, which increases Ids and so on. The Rg maximum value to avoid thermal runaway is defined experimentally and is fortunately considerably higher than the value, 6 ohms, already defined.

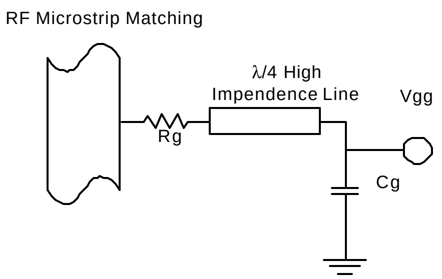


Figure 1A. Typical Gate damping circuit

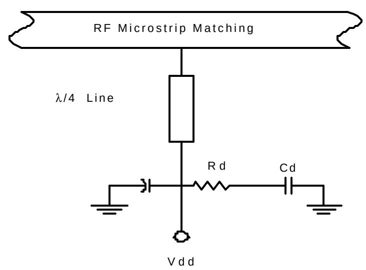


Figure 1B. Typical Drain damping circuit

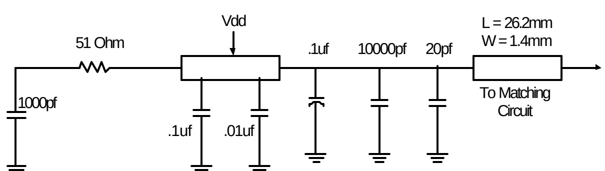


Figure 2. Gate bias network

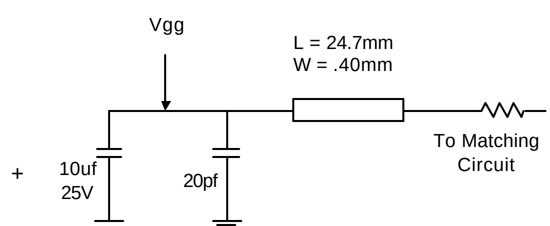


Figure 3. **Drain bias network**

Drain Bias Circuit

The drain bias circuit has several functions:

- To maintain a constant Drain-to-Source voltage up to Ids maximum, 20A typical, under drive.
- To supply Drain current at least up to Ids maximum under drive.
- To stabilize the device for the frequencies out of the amplifier bandwidth.
- To filter the signal and the products generated by the device from low frequencies to high frequencies. It should be noted that the drain biasing circuit could be an element of the output matching circuit.
- Isolate the Gate from any signal from the device output to minimize the Gate-to-Drain coupling through biasing connections.

Figure 1B and Figure 3 show the amplifier drain biasing circuit. It consists of a quarter-wave length microstrip line connected at one end to the output matching circuit and at the opposite end short-circuited by several capacitors. These capacitors consist of several values and types: a small value, few pF, very high Q, to realize a good RF short circuit in the amplifier RF passband, then 100 pF, 1, 10, 100 nF (ceramics), 1 and 10 uF (Tantalums) to realize a good filtering (short circuit to the ground) from very low frequencies up to the fundamental frequency. Capacitors with low parasitic series inductance and resistance should be used. Not all values are required for every application. In addition to these capacitors a resistor, Rd, in series with a capacitor, Cd, is connected to the extremity to the line to the ground. This circuit brings a dissipating element in parallel to the capacitors and improves the stability of the amplifier. The quarter-wave length microstrip line cannot have a very high impedance since it has to carry a relatively high current when the device is in compression, up to 20A typical.

The bias networks shown in Figures 2 and 3 utilize the techniques described above. The circuit board layouts are included in Figures 7a and 7b.

RF Matching with Balanced Devices

FLL1500IU-2C RF Parameters

The 2.11-2.17 GHz frequency band input and output half device impedances for optimal WCDMA ACPR performance are provided in the following table. The bias conditions associated with these impedances are V_{DS} = 12V and I_{DSQ} = 2A each side.

The approach (see figure 4) is to measure the device optimal input impedance, Zin, for gain and the device optimal output impedance, Zout, for power (or IM3 or ACPR as desired). Unfortunately these parameters cannot be measured directly. So actually the impedances connected to the device ports to achieve optimal performance, Zsource at the input and Zload at the output, are measured.

And, by definition,

Zin = Zsource* and

Zout= Zload*.

One side (half of the device) is measured at a time. Zin and Zout are the input and output impedances when simultaneously Zin is optimized for gain and Zout for output power ($Zout|_{power}$) or IMD3 ($Zout|_{IM3}$) or ACPR ($Zout|_{ACPR}$). Note that the output impedances are typically close in value but not identical.

Table 2. Single Ended Device Impedances (Gate-to-Ground, Drain-to-Ground) Zin for gain and Zout for ACPR. at Pout=10 W

Frequency	$Zin|_{GAIN}$ (Ohm)		$Zout|_{ACPR}$ (Ohm)	
GHz	Real	Imag.	Real	Imag.
2.11	14.2	11.5	37.2	17.7
2.14	13.6	11.5	34.1	18.6
2.17	12.9	11.5	31.3	19.0

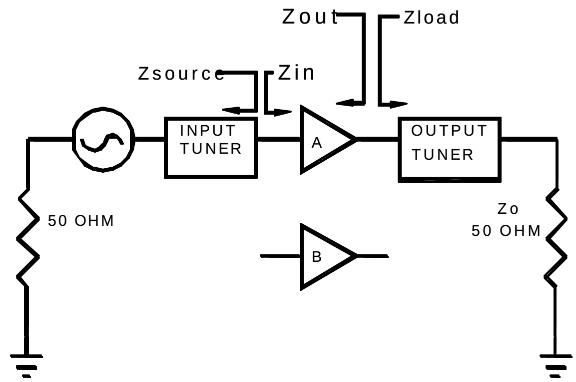


Figure 4.Source/Load-pull measurement method and definitions

Balanced Circuit Design Approach

The input and output 3-dB quadrature couplers (see figure 5) are purchased surface-mount 4 port devices. The RF signal is applied to any one port of the coupler. If we call this port 1, and number the ports clockwise around the part, then port 2 is the coupled port, port 3 is the through port, and port 4 is the isolated port. Energy is coupled to port 2, and the remainder is transmitted to port 3. In the case of a 3-dB coupler considered here, the two signals are equal in amplitude. Port 2 leads port 3 in phase by 90 degrees. The energy at port 4 is decreased by the isolation of the coupler, typically 20 dB

Each of the two signals is amplified by one of the two sides of the device, which are DC and RF matched chips, from the same wafer. Unfortunately, spurious due to the non-linearity of the device are also produced in the devices. The two signals with their associated spurious propagate to the output coupler. The same phase shift and signal splitting occurs for each of the signals at the output as occurred in the input coupler. The resulting voltages for the signal and odd order products in the amplifier band of interest such as 2F1-F2 and 2F2-F1 are summed in the load and cancelled in the isolated coupler port. This process is illustrated in Figure 5.

Input Matching Network

The input matching circuit for each device side was optimized for return loss at 2.14 GHz. Due to the narrow bandwidth of this application and the low Zin and Zout

Q, a single frequency match is sufficient, though the full band was monitored to verify good match over the 2.11-2.17 GHz band. The impedances were entered into a file and matched using Touchstone Linear Analysis program, in this case a part of HPADS. Any linear analysis tool will do to determine an optimum match. In the input device plan a parallel open-circuited stub to cancel the input susceptance of the device admittance was connected. Then a quarter-wave transformer was inserted to transform the real impedance, 37 ohms, resulting from the stub connection, to 50 ohms. The final amplifier circuit consists of two identical microstrip lines and tuning parallel stubs, one for each side. The DC blocking capacitors were placed close to the first matching element. A gate feed was placed as close to the plane of the gate as possible, with a resistor in series with a quarter-wave high impedance line leading to an RF short. This yielded an open circuit at the fundamental frequencies

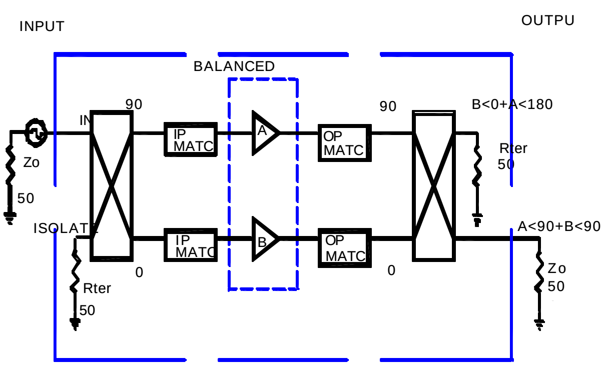


Figure 5. Representation of Balanced Matching

Output Matching Network

The output matching circuit for each device side was optimized for ACPR performance at 2.14 GHz. Match for optimum output power/power-added efficiency performance is to a slightly different impedance from that for WCDMA (Wideband Code Division Multiple Access) Adjacent Channel Power Ratio (ACPR) performance or for optimum IMD performance. The selected impedances were entered into a file and matched using Touchstone Linear Analysis program, in this case a part of HPADS. Any linear analysis tool will do to determine an optimum match. An open-circuited parallel stub was connected in the output plane of the device to cancel the output susceptance of the device admittance. Then a quarter-wave transformer was inserted to transform the real impedance, 60 ohms, obtained after the stub, to 50 ohms. A quarter-wave drain feed was placed as close to the plane of the device drain as possible. The high current levels in the drain circuit require a drain feed circuit with relatively large trace width. A 50-ohm impedance (W=2 mm) line was used. This yielded an open circuit at the fundamental frequencies, and a short at the second harmonic.

Large-Signal Circuit Tuning

The best load/source pull parameters are only accurate to within about 10 percent. Therefore to obtain optimum results, some re-tuning is necessary, in particular with respect to the output circuit. The reverse gain, S_{12} , of the FLL1500IU-2C 150-Watt device is high enough to require re-tuning of the input circuit once the output match has been changed. The FLL1500IU-2C internal pre-matching circuit made optimum external tuning easy to achieve. Once the tuning was found, consistent performance was observed versus devices from different lots. The results reported are for data taken from 5 devices from 3 lots after tuning for the first device in the set.

Note that the location for the optimal match to get optimum output power and power-added efficiency was different from the optimal match for WCDMA (Wideband Code Division Multiple Access) Adjacent Channel Power Ratio (ACPR) performance. The Output power was less than the rated value for the device as a result. Tuning for power returned the output power to the full rated value at the cost of a couple dB of ACPR performance. Optimal match was different again for optimum 2-tone CW IMD3 performance. Tuned input and output circuits for WCDMA ACPR performance are shown, Figures 6 through 8.

Device Maximum Power Dissipated Versus Flange Temperature

The maximum power dissipated, Pdiss. by the device is limited by the maximum recommended channel temperature, which is 175^{O}C. It is important for the amplifier designer to be able to calculate the maximum Pdiss for their applications. This calculation is not as simple as it may appear since the thermal resistance of a GaAs device is a strong function of the device-flange temperature (Tf) and the channel temperature (Tch) or Pdiss. The FLL1500IIU-2C data sheet and the article "Understanding Thermal Basics For Microwave Power Devices"[(2)] allow the designer to calculate the device thermal resistance (Rth) versus Tf and Tch or Pdiss. It means by knowing Rth1 for one set of the parameters (Tf1 & Tch1), Rth2 can be calculated for another set of parameters (Tf2, Tch2 or Pdiss2). The formulas are derived from the Kirchoff's transformation and the variation of the GaAs thermal conductivity versus temperature. Because the flange thermal resistance (Rthf) is constant, it has to be subtracted from the global Rth before applying the correction.
We have assumed Rthf=0.3xRth=0.165 K/W.
The initial values are from the device data sheet: Tf1=25^{O}C, Tch1=25+0.55x12x4=51.4^{O}C, Rth=0.55 K/W, Rthf =0.165 K/W. From these values, the maximum Pdiss can be calculated versus Tf for Tch=175^{O}C. If the device is operated at low signal, the worst case is when there is no input signal and table 3 gives Idsq maximum versus Tf. If the device is operated only in compression then Pdiss maximum should be used and calculated with the following formula:

$$\text{Pdiss.}=(\text{VdsxIds})+\text{Pin}-\text{Pout} \qquad (\text{W})$$

Device Attachment

Another thermal issue is the device attachment between the part flange and the housing. The device must be in good thermal contact with the heat sink.
A good heat exchanger to the ambient environment is also important but beyond the scope of this article.
As each application has a unique set of system requirements relating to size, construction and environmental conditions, these parts of the thermal design are left to the user.

Table 3. Thermal Impedance and Max Power/Quiescent Current Example for Rth nominal = 0.55 K/W

Tf (^{O}C)	Tch (^{O}C)	Rth (^{O}K/W)	Max. Pdiss. (W)	Max Idsq at 12 V (A)
0	175	0.649	269.5	22.5
10	175	0.656	251.7	21.0
20	175	0.662	234.1	19.5
30	175	0.669	216.9	18.1
40	175	0.675	200.0	16.7
50	175	0.682	183.4	15.3
60	175	0.688	167.2	13.9
70	175	0.694	151.2	12.6
80	175	0.701	135.6	11.3
90	175	0.707	120.2	10.0
100	175	0.714	105.0	8.8

Impedance parameter files

These are the impedance 1-port files for matching created from table 2 impedances. Listing is in Touchstone format.

The impedance parameter file for the input Zin:

"FLL1500IU2C_Zin_an.S1P"

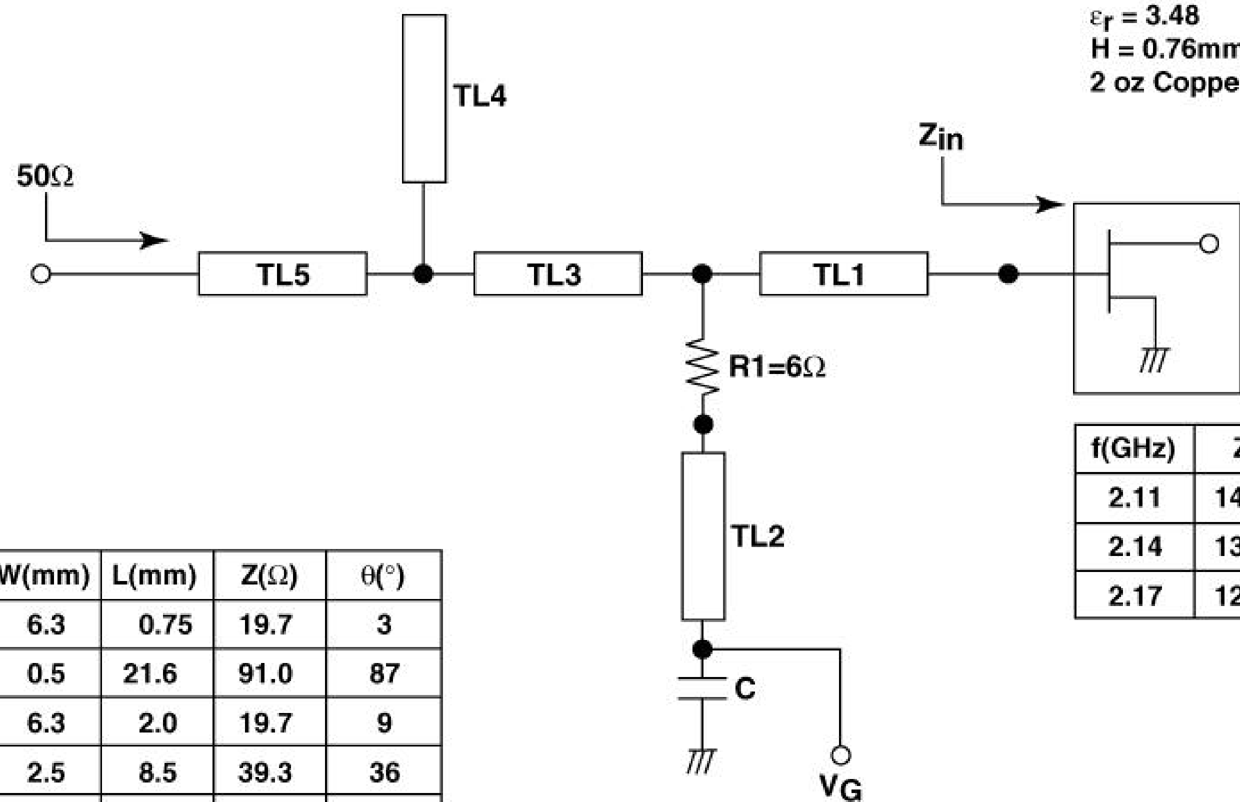
```
!Zin for FLL1500IU-2C measured at 12 V 4 A
!Frequency
# GHz RI R 50
! Freq   Real    Imaginary
2.11     0.284   0.23
2.14     0.272   0.23
2.17     0.258   0.23
```

The impedance parameter file for the output Zout:

"FLL1500IU2C_Zout_an.S1P"

```
!Zout for FLL1500IU-2C measured at 12 V 4 A
!Frequency
# GHz RI R 50
! Freq   Real    Imaginary
2.11     0.863   0.293
2.14     0.702   0.075
2.17     0.74    0.038
```

Board: Rogers 4350 or Equiv.
$\varepsilon_r = 3.48$
H = 0.76mm(.031in)
2 oz Copper

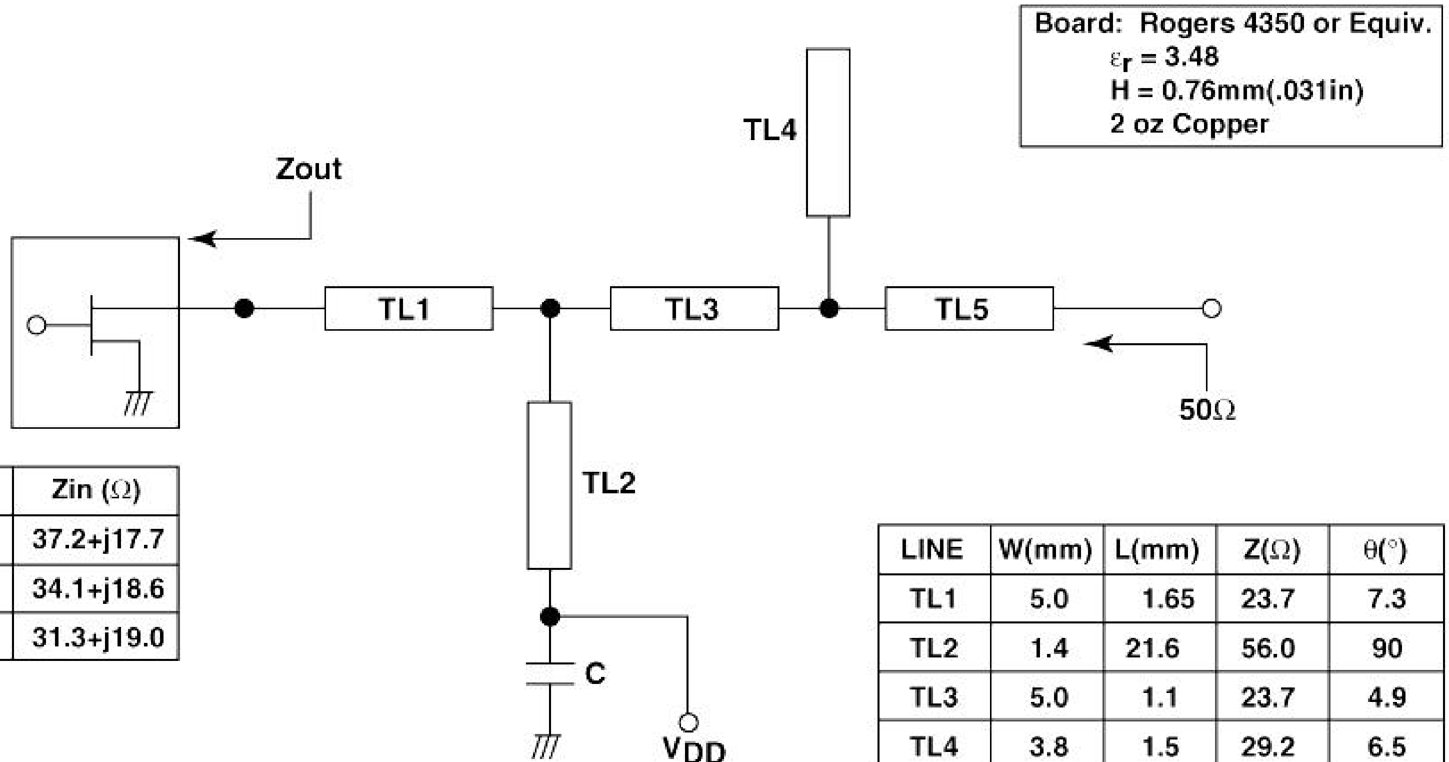


f(GHz)	Zin (Ω)
2.11	14.2+j11.5
2.14	13.6+j11.5
2.17	12.9+j11.5

LINE	W(mm)	L(mm)	Z(Ω)	θ(°)
TL1	6.3	0.75	19.7	3
TL2	0.5	21.6	91.0	87
TL3	6.3	2.0	19.7	9
TL4	2.5	8.5	39.3	36
TL5	2.5	21.5	39.0	92

θ = Electrical Length at f = 2.14GHz

Figure 6. SIMPLIFIED INPUT MATCHING CIRCUIT FOR FLL1500IU-2C BALANCED AMPLIFIER (2.11-2.17GHz)



f(GHz)	Zin (Ω)
2.11	37.2+j17.7
2.14	34.1+j18.6
2.17	31.3+j19.0

LINE	W(mm)	L(mm)	Z(Ω)	θ(°)
TL1	5.0	1.65	23.7	7.3
TL2	1.4	21.6	56.0	90
TL3	5.0	1.1	23.7	4.9
TL4	3.8	1.5	29.2	6.5
TL5	1.7	22.2	50.0	94

θ = Electrical Length at f = 2.14GHz

Figure 7. SIMPLIFIED OUTPUT MATCHING CIRCUIT FOR FLL1500IU-2C BALANCED AMPLIFIER (2.11-2.17GHz)

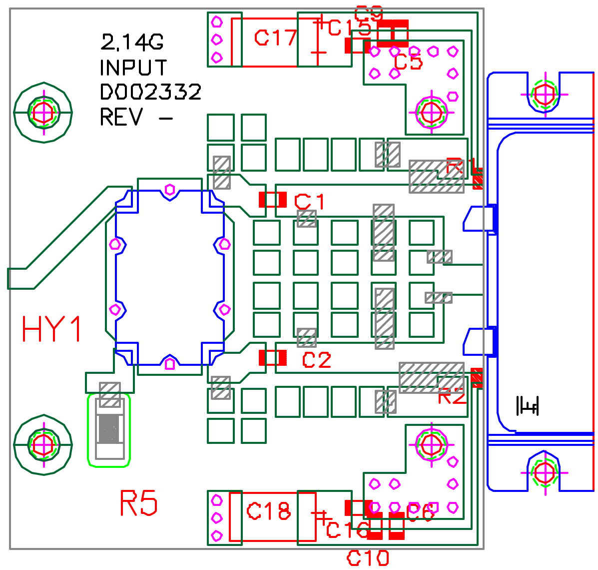


Figure 8A. Amplifier Input Match Circuit Optimized for Gain Performance

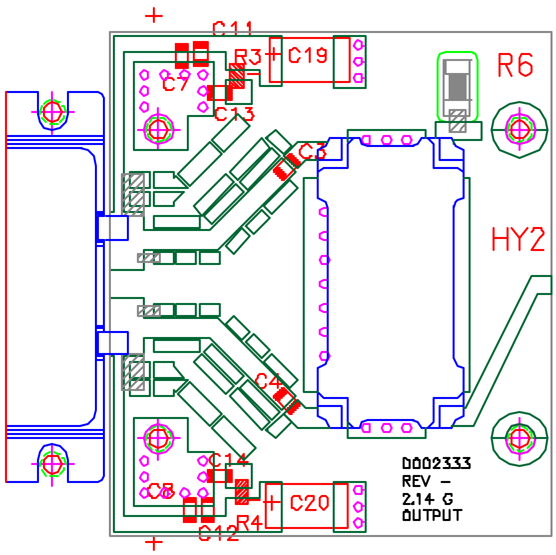


Figure 8B. Amplifier Output Optimized for WCDMA ACPR Performance

REF DES	VALUE	COMMENTS
C1–C8	4.7pf	ATC case A; 0603 hi Q
C13–C16	.01uf	
C9–C12	1000pf	
C17–C20	10uf	
R1, R2	10 ohm	
R3–R4	51 ohm	
R5,R6	50 OHM	DDC100200AG50RD OR EQ
HY1	IP CPLR	1A1306-3
HY2	OP CPLR	503B2150N2

Figure 8C. Amplifier Parts List

Measured Results

The performance obtained with the FLL1500IU-2C using the circuitry of Figures 7 and 8 is presented in the following graphs. The amplifier was tuned for optimum WCDMA ACPR at 2.14 GHz at a target output power of 43 dBm with Vdsq = 12V and Idsq=4A total. No RF tuning changes were made for CDMA measurements at other bias settings or those for IMD. The WCDMA signal source was an HP 4433B system, (WCDMA signal configuration: 4.096 MHz BW @ 5 MHz offset, 1 PERCH +50 DTCH). ACPR was measured using HP8562A Spectrum Analyzer and 'Delta Marker Method' with a resolution bandwidth of 100 KHz and a video bandwidth of 100 Hz.

Figure 9 shows output power and power-added efficiency performance versus input power.

Figure 10 shows the output power and power-added efficiency versus frequency response.

Figure 11 shows Third order intermodulation performance for two CW tones versus total output power.

Figure 12 provides WCDMA ACPR data versus total output power at three frequencies.

Figure 13 shows the results of life testing for the device class.

In order to provide the optimum performance for a specific bias point, the RF tuning may need to be adjusted.

Conclusion

This application note has provided the circuit designer with a design for a 150-W balanced amplifier that provides a WCDMA ACPR performance of -41 dBc typical at output power level of 20 W (43.0dBm) for WCDMA base station applications.

Notes

(1). J. Shumaker, R. Basset and A. Skuratov, "High-Power GaAs FET Amplifiers: Push-Pull versus Balanced Configurations. Example WCDMA (2.11-2.17 GHz), 150-W Amplifiers," Wireless Symposium 12-16 February 2001.

(2): R. Basset, "Three Balun Designs For Push-Pull Amplifiers", Microwaves, July 1980, page 47-52.

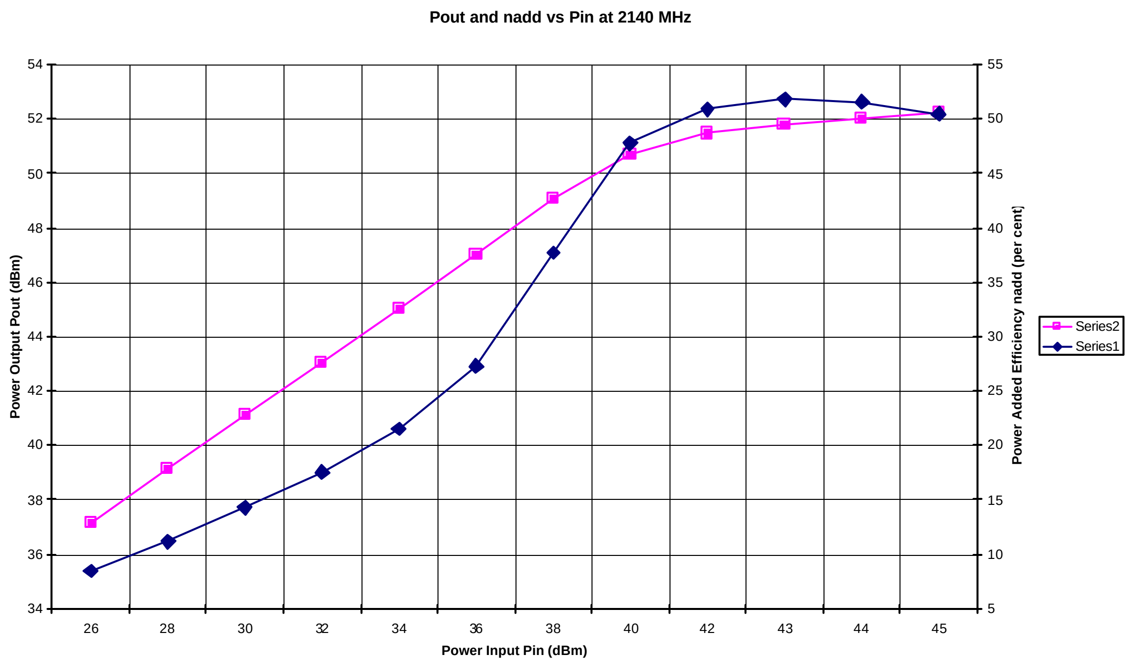


Figure 9. Output Power and Power Added Efficiency vs. Input Power (tuned for WCDMA ACPR @ Ids=4A)

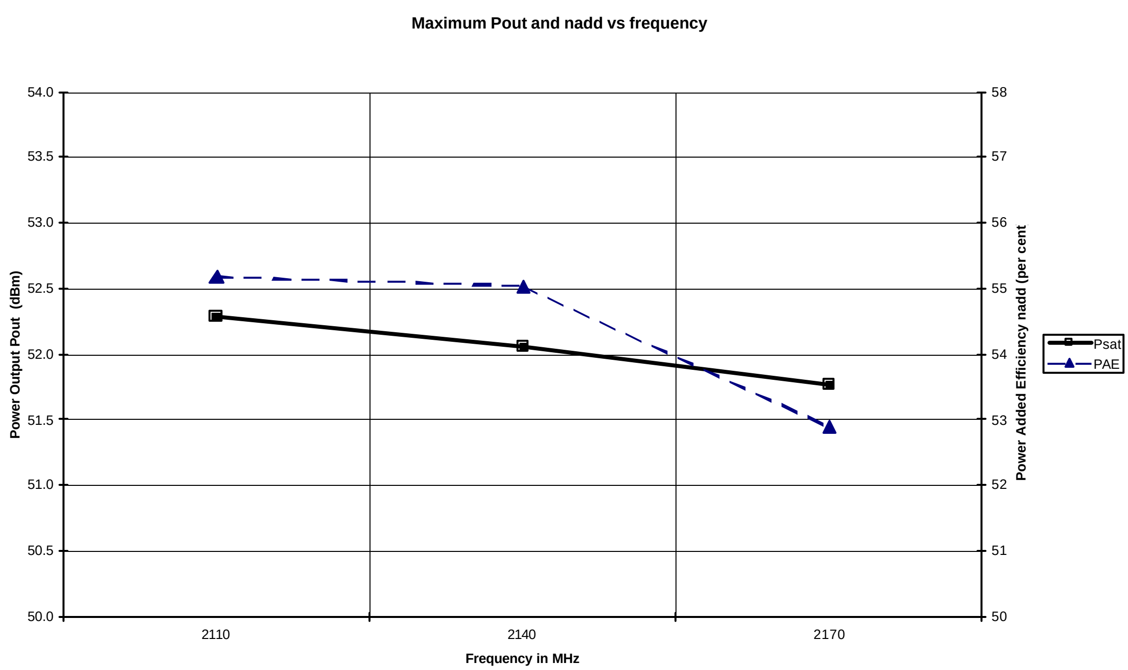


Figure 10. Maximum Output Power and Power Added Efficiency vs. Frequency (tuned for WCDMA ACPR @ Ids=4A)

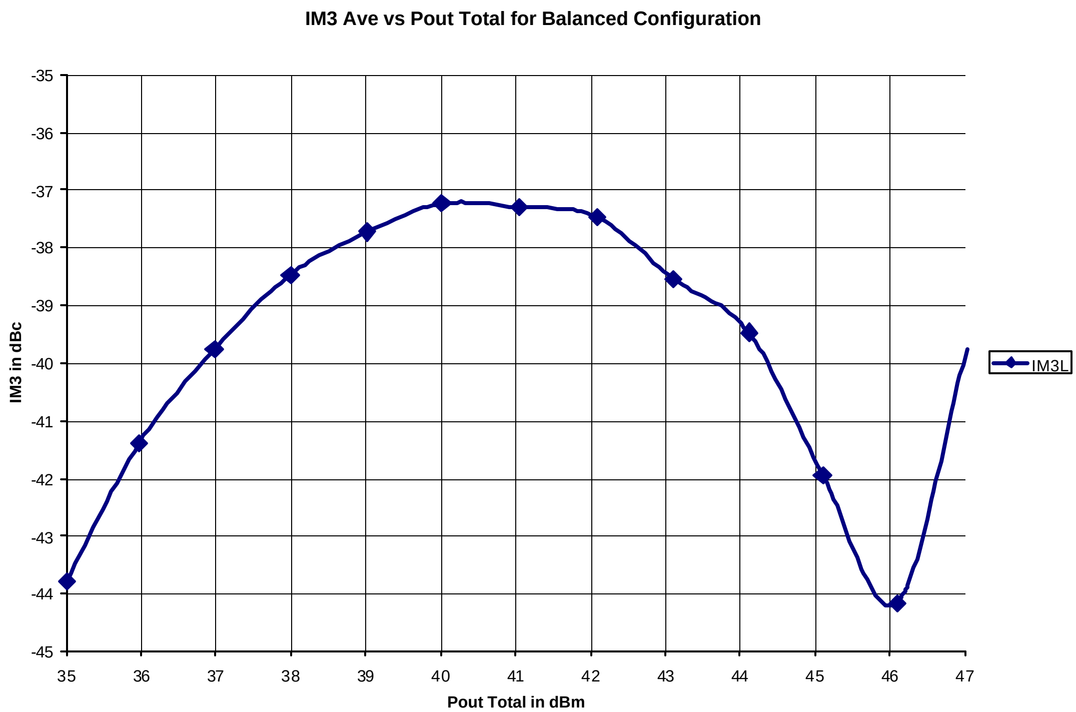


Figure 11. Two CW Tone Intermodulation Ration vs. Output Power (tuned for WCDMA ACPR @ Ids=4A)

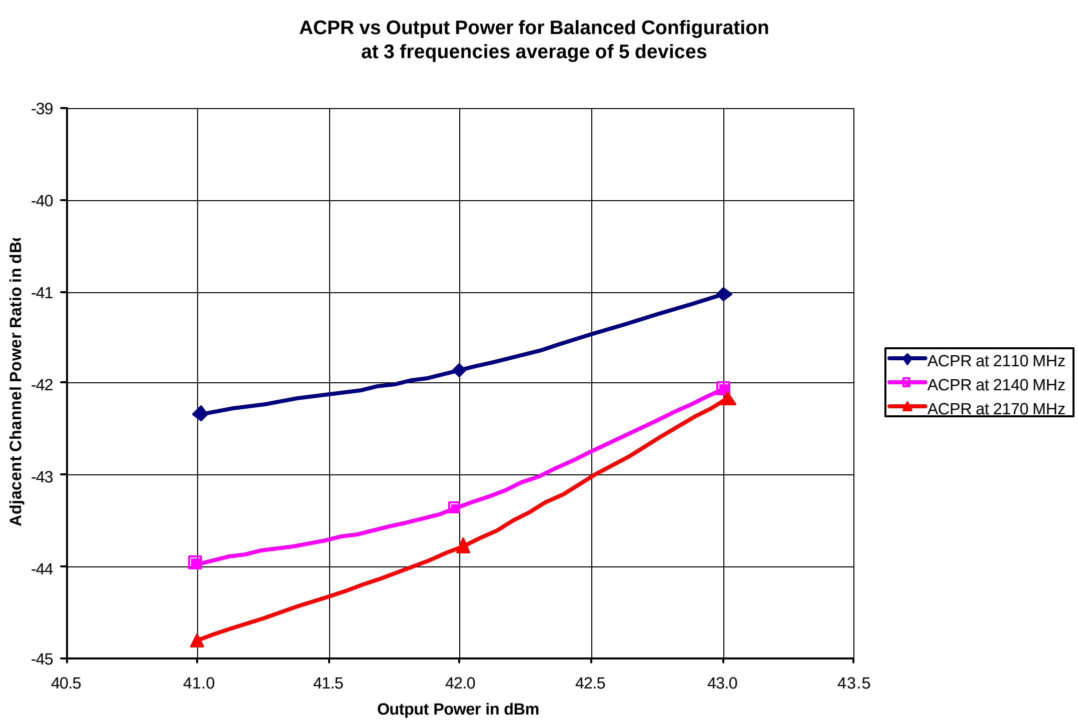


Figure 12. ACPR versus Output Power at 3 frequencies (tuned for WCDMA ACPR @ Ids=4A)

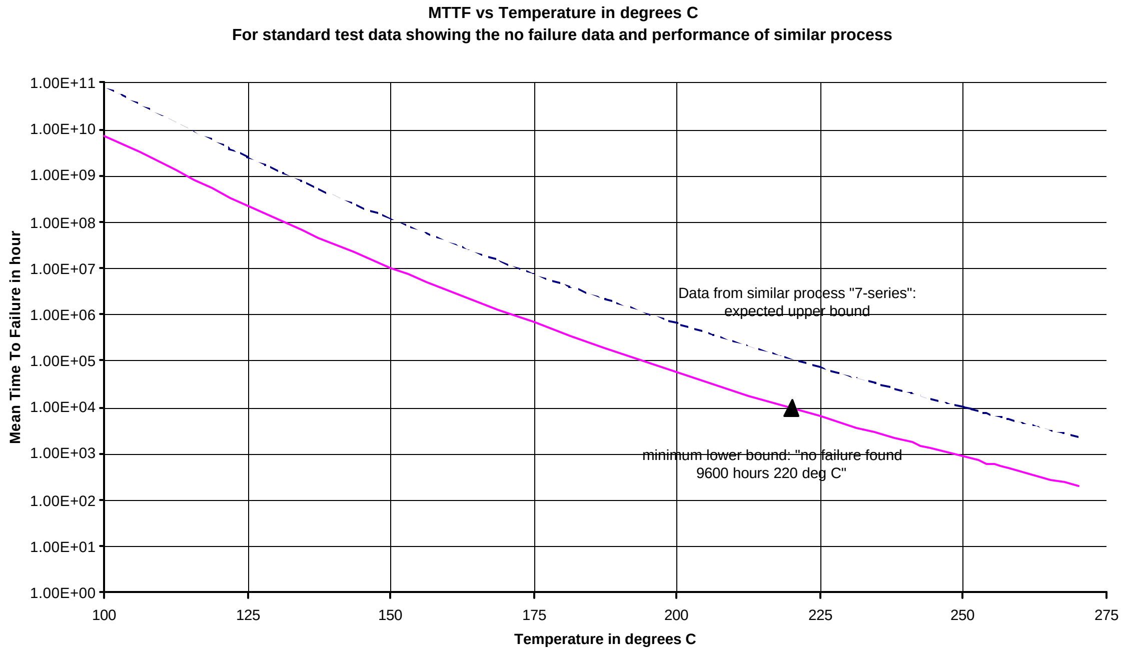


Figure 13. Reliability Curve of MTTF vs Temperature for Device Class

FLL1500IU-2C Device Data

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta=25°C)

Parameter	Symbol	Condition	Rating	Unit
Drain Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T	Tc = 25°C	187.5	W
Storage Temperature	T_{stg}		-65 to +175	°C
Channel Temperature	T_{ch}		+175	°C

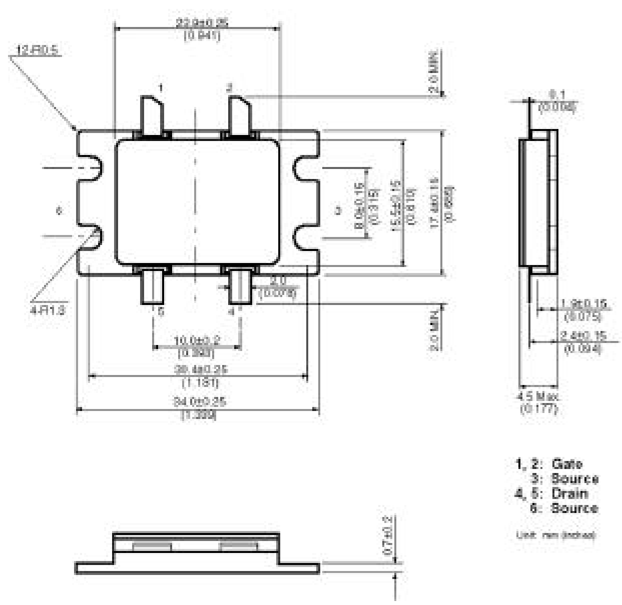
Fujitsu recommends the following conditions for the reliable operation of GaAs FETs:

1. **The drain-source operating voltage (V_{DS}) should not exceed 12 volts.**
2. **The forward and reverse gate currents should not exceed 353mA and –-103.6mA respectively with Gate resistance of 10W**
3. **The operating channel temperature (Tch) should not exceed +145° C.**

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0V	-	16	-	A
Pinch-Off Voltage	V_p	V_{DS} = 5V, I_{DS}=440mA	-0.1	-0.3	-0.5	V
Gate-Source Breakdown Voltage	V_{GSO}	I_{GS} = -4.4 mA	-5	-	-	V
Output Power	P_{out}	V_{DS} = 12V F=2.17 GHz I_{DS} = 4.0A Pin=43.0 dBm	50.8	51.8	-	dBm
Linear Gain	GL		11.0	12.0	-	dB
Drain Current	I_{DSR}		-	23	30	A
Power-Added Efficiency	h_{add}		-	48	-	%
Thermal Resistance	R_{th}	Channel to case	-	0.55	0.8	°C/W

Case Style "IU"



FUJITSU