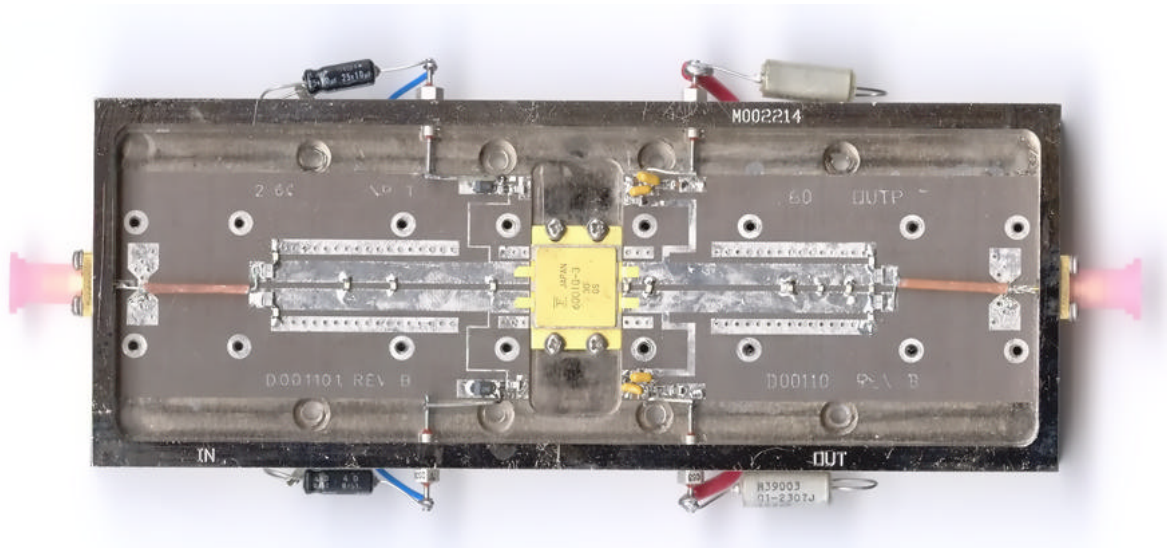


FUJITSU APPLICATION NOTE - No 007

60-W, 2.5- 2.7 GHz Push-Pull Amplifier For MMDS Base-Station Application Using The FLL600IQ-3 GaAs FET Device



FEATURES

- Targeted WCDMA ACPR at 6 W average
- Over 60 Watts P_{out} over entire band
- High gain
- Good repeatability
- Easy tuning for Power, WCDMA ACPR, and IMD
- High MTTF > 10^6 hours @ $T_{CH} = 175^\circ C$
- High linearity
- High Power-Added Efficiency

SUMMARY: A 60-W push-pull amplifier design for the 2.5-2.7 GHz MMDS band using the Fujitsu FLL600IQ-3 GaAs FET device is presented. Full circuit design details as well as the measured results for class A-B operation are provided. Information required for balanced amplifier design is provided without example.

Circuit Description

The circuitry described in this application note provides the microwave engineer with a design for a 60-Watt push-pull amplifier. This design is suited for WCDMA applications requiring high linearity and efficiency. The high linearity is obtained with a minimum of matching components. The amplifier can operate over the entire 2.5-2.7 GHz MMDS band. WCDMA ACPR performance of -45 dBc typical has been obtained at 6 W (38 dBm) average output power.

Push-Pull vs. Balanced Configuration Approach

Both push-pull and balanced configurations⁽¹⁾ result in a similar basic performance when operated in any class of operation and in bandwidth smaller than one octave. Both can be designed for similar linearity and efficiency performance as an amplifier for commercial application with relatively narrow bandwidth (10%). However the balanced approach has the following advantages in system use.

- Better stability
- Better external match
- Good isolation between the two identical sides of the device
- Ease to design quadrature couplers and to integrate them to the amplifier layout

The example presented today will be that of the push-pull circuit.

Amplifier Components

The RF circuit elements of the 60W amplifier are the Fujitsu FLL600IQ-3, 60-W power GaAs FET device, two 50-ohm coaxial baluns⁽²⁾, several capacitors and resistors mounted on a dielectric substrate. A detailed parts list can be found in Figure 7.

FLL600IQ-3 Device Description

The FLL600IQ-3 utilizes two 30-W Au gate power GaAs FET chips that are independently configured within the Fujitsu IQ package. Internally pre-matching networks are used for each side of the device to raise the input and output impedances of the chips to allow for easier external matching circuit design. The 0.6μm Au gate FET chip has an MTTF of 1x10⁸ hours for a channel temperature of 150°C, at the overvoltage condition of 15V drain-to-source. For those who need to calculate reliability at other temperatures, the activation energy for this transistor type has been measured at Ea=1.79 eV, and the life extrapolated from measured data. See Figure 13 at the end of the data section. The FET chips and the IQ package give a thermal resistance of typically 0.8 K/W. Additionally, the IQ package is hermetically sealed for applications where extreme environmental conditions may be encountered.

Balun and Board Material Description

The 2.5–2.7GHz, 60-W linear amplifier design presented in the following sections is achieved by using 50-ohm coaxial baluns⁽²⁾ and an Arlon 522T0311160, 2.6 dielectric constant (ϵ_r) substrate. All components used in the design are commercially available. The substrate's physical and electrical parameters are summarized below.

ϵ_r	h, mm	Metallization type	Thickness mm
2.60	.787	Cu	.034

Table 1. Arlon substrate parameters

DC Bias Circuit Topology

Gate Biasing Circuit

The gate biasing circuit has several functions:

- To maintain a constant gate-to-source voltage .
- To be able to supply a negative and positive gate current.
- To protect the gate by limiting the gate current when the device goes in breakdown (drain-to-

gate or gate-to-source) or when the gate-to-source junction is biased with a positive voltage. These abnormal operating conditions for the devices can be due to an operator error, an overdrive, a system problem or ESD.

- To stabilize the device in case a negative resistance appears in the gate at any frequency where the device has gain.
- To filter the signal and the products generated by the device input circuit from very low frequencies to high frequencies without affecting the device input matching circuit.
- Isolate the gate from any signal coming from the drain, to minimize the coupling gate-to-drain (feedback) at any frequency where the device has a gain.

Figure 1A shows the generic amplifier gate biasing circuit, and figure 2 shows the circuit in more detail. Starting from the input matching circuit, it consists of a gate resistor, R_g , connected to the input of a quarter-wave length high impedance microstrip line short-circuited at its extremity by a several capacitors. The impedance of the biasing circuit connected in parallel to the input matching circuit is very high since it is a resistor in series with a quarter-wave short-circuited high impedance microstrip line. Thus the resistor and bypass have no effect on the input matching circuit.

Several capacitors are connected at the extremity of the quarter-wave length line. The complete case starts with a small value, few pF, to realize a good RF short circuit in the amplifier RF passband, then 100 pF, 1, 10, 100 nF, 1 and 10 uF to realize a good filtering (short circuit to the ground) from very low frequencies up to the fundamental frequency. Capacitors with low parasitic series inductance and resistor should be used. Not all values are required for every application.

Since the average current in the gate, I_{gs} , is relatively low (absolute value is less than 50 mA), the current handling of the gate bias circuit doesn't have to be higher than 100 mA. It means a high impedance transmission line can be used.

The value of the gate resistance is a compromise between minimum and maximum limits.

Minimum Resistance Limit

- Low Frequency Stabilization: The bias resistor should be connected as close as possible to the gate. For relatively low frequencies, the DC blocking capacitors (picofarads) are open circuits, the decoupling capacitors (microfarads) are short circuits and the quarter-wave lines at RF frequencies become short lines. It means for low frequencies, the gates are connected to the ground through the gate resistors. If a negative resistance ($R < 0$) appear in the gates and the sum of the resistors ($R + R_g > 0$) is positive the device will be stable. This function requires R_g to have a sufficient value and the connection to the ground to be short for low frequencies. Connecting the resistor close to the gate reduces the connection length to the ground .
- The gate current limitation under breakdown, large drive and EDS requires a sufficient R_g value but this value for the below reasons has to be limited.

Maximum Resistance Limit

- The gate voltage, V_{gs} , should be maintained constant versus the drive level i.e. versus I_{gs} . The gate current, I_{gs} , versus drive can change from -2 to 80 mA typical. If the desired V_{gs} maximum variation versus drive is about 200 mV, the maximum value of R_g is $R_{gMax} = 200/80 = 3$ ohms total. It means 6 ohm resistor maximum for each side of the device.
- The device thermal runaway limits also the maximum value of R_g . The runaway mechanism can be explained as follows. $V_{gs} = V_{gg} - I_{gs} * R_g$, with I_{gs} negative without RF drive. Thus when the temperature increases, I_{gs} becomes more negative and V_{gs} increases. This increase of V_{gs} increases I_{ds} , which increases the power dissipated in the device i.e. the channel temperature. The channel temperature rise makes I_{gs} more negative, which increases I_{ds} and so on. The R_g maximum value to avoid thermal runaway is defined experimentally and is fortunately considerably higher than the value, 6 ohms, already defined.

RF Microstrip Matching

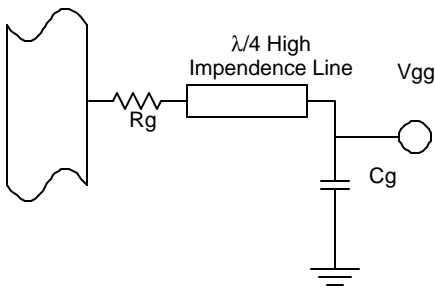


Figure 1A. Conceptual Gate bias circuit

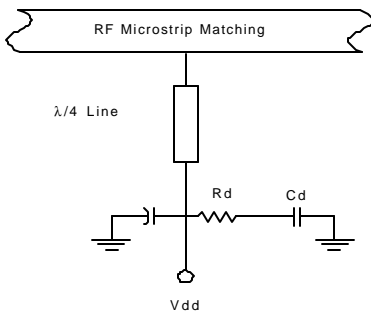


Figure 1B. Conceptual Drain Bias circuit

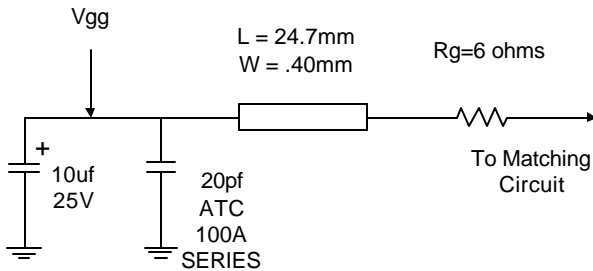


Figure 2. Gate bias network

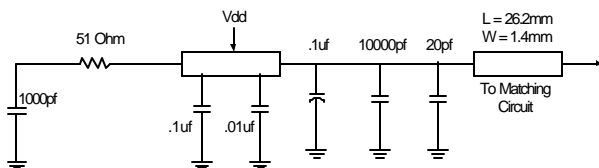


Figure 3. Drain bias network

Drain Bias Circuit

The drain bias circuit has several functions:

- To maintain a constant Drain-to-Source voltage up to I_{ds} maximum, 11A typical, under drive.
- To supply Drain current at least up to I_{ds} maximum under drive.
- To stabilize the device for the frequencies out of the amplifier bandwidth.
- To filter the signal and the products generated by the device from low frequencies to high frequencies. It should be noted that the drain biasing circuit can be an element of the output matching circuit.
- Isolate the Gate from any signal from the output circuit to minimize the Gate-to-Drain coupling.

Figure 1B and Figure 3 show the amplifier drain biasing circuit. It consists of a quarter-wave length microstrip line connected at one end to the output matching circuit and at the opposite end short-circuited by several capacitors. In the complete case, these capacitors consist of several values and types: a small value, few pF, very high Q, to realize a good RF short circuit in the amplifier RF passband, then 100 pF, 1, 10, 100 nF (ceramics), 1 and 10 uF (Tantalums) to realize a good filtering (short circuit to the ground) from very low frequencies up to the fundamental frequency. Capacitors with low parasitic series inductance and resistance should be used. Not all values are required for every application. In addition to these capacitors a resistor, R_d , in series with a capacitor, C_d , is connected to the extremity to the line to the ground. This circuit brings a dissipating element in parallel to the capacitors and improves the stability of the amplifier. The quarter-wave length microstrip line cannot have a very high impedance since it has to carry a relatively high current when the device is in compression, 11 A typical.

The bias networks shown in Figures 2 and 3 utilize the techniques described above. The circuit board layouts are included in Figures 7a and 7b.

RF Matching with Push-Pull Devices

FLL600IQ-3 Source/Load-Pull Parameters

The MMDS frequency band single-ended device input and output impedances for optimum WCDMA ACPR performance are provided in the following table. The bias conditions associated with these impedances are $V_{DS} = 12V$ and $I_{dsq} = 2A$ each side.

The approach (see figure 4) is to measure the device optimal input impedance, Z_{in} , for gain, and the device optimal output impedance, Z_{out} , for power (or IM3 or ACPR as desired). Unfortunately the parameters cannot be measured directly. So actually the impedances connected to the device ports to achieve optimal performance, Z_{source} at the input and Z_{load} at the output are measured.

An by definition,

$$Z_{in} = Z_{source}^*$$

$$Z_{out} = Z_{load}^*$$

One side (half of the device) is measured at a time, see figure 4. Z_{in} and Z_{out} are the input and output impedances when simultaneously Z_{in} is optimized for gain and Z_{out} for for output power ($Z_{out}/power$) or for ACPR ($Z_{out}/ACPR$). Note that $Z_{out}/power$ and $Z_{out}/ACPR$ impedances are close but not identical.

Table 2. Device Impedances, taken one side at a time (Single-Ended: Gate-to-ground, Drain-to-Ground). $V_{ds}=12V$, $I_{dsq}=2A$ each side. 60-W Device Optimum Input and Output Impedances

Frequency GHz	Z_{IN} (Ohm)		Z_{OUT} (Ohm) Power match		Z_{OUT} (Ohm) ACPR match	
	Real	Imag.	Real	Imag.	Real	Imag.
2.5	16	8.3	9.5	3	7.4	11.5
2.6	11.9	8.5	9.5	-1.25	8.4	9.8
2.7	11.2	14.6	6.9	-3.3	14.4	3.8

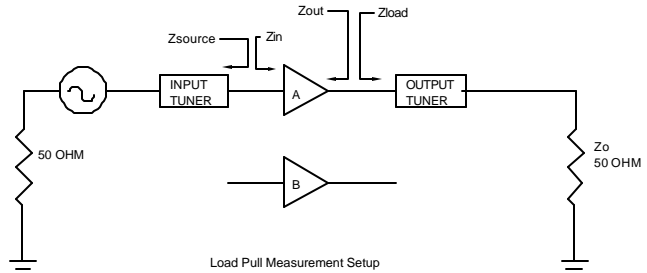


Figure 4. Source/ Load-pull measurement method and definitions.

Push-Pull Circuit Design Approach

The input and output baluns⁽²⁾ (see figure 5 A thru C) consist of a 50-ohm semi-rigid coaxial whose unbalance extremity is connected to a 50-ohm microstrip line and whose its balanced ports are connected to two 25-ohm microstrip lines. For simplicity it will be assumed that this balun is perfectly symmetric and has no leakage ($Z_{leakage}$ is infinite) to the ground. This is not fully true since no symmetrizer was used and the leakage impedance ($Z_{leakage}$) due to the external coaxial conductor connected to one of the balanced port (external coaxial conductor) is not an infinite impedance. However $Z_{leakage}$ in the amplifier band is considerably higher than the 25-ohm impedance.

The electrical length (θ) of the baluns has no effect on the matching since this 50-ohm line is connected to 50-ohm impedance at its unbalanced port and at 2x25-ohm impedance at its balanced ports. Only the electrical length (θ') of the line consisting of the coaxial external conductor and the ground is important and should be close to quarter-wave length.

We will consider for modeling purpose only half the push-pull amplifier (see figure 5A for an idealized schematic). Each side of the device (half the device) has to be matched to 25-ohm impedance. It means the half device input impedance (Z_{in}) and output impedance (Z_{out}) have to be matched to 25-ohm impedance. Figure 5B extends the model to both device halves and includes the baluns at the input and output used to get to 50-ohm impedance. Figure 5C extends the model to the practical amplifier.

Input Matching Network

The input matching circuit for each device side was optimized for flat gain over the 2.5-2.7 GHz band and to provide a perfect match to 25-ohm impedance at 2.7 GHz. The final amplifier circuit (see figure 5C) consists of two identical parallel microstrip lines and chip capacitors mounted between these two lines. Because a virtual ground exists between the two lines, it is not necessary to connect shunt impedances to ground. When using the virtual ground the impedance is doubled, so the capacitor values are half the single ended design value.

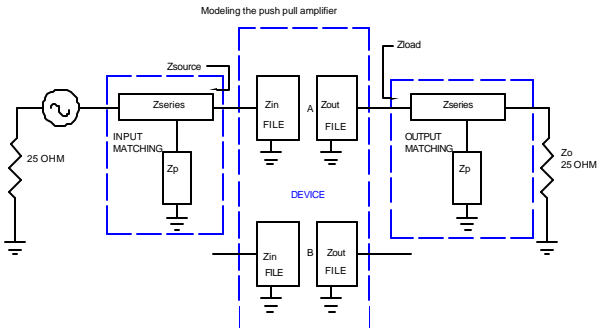


Figure 5A. Representation of Push-Pull matching

Output Matching Network

The output matching circuit was optimized for 2 tone ACPR (2 W-CDMA signals 10 MHz apart, modulated at 4.096 MHz BW @ 5 MHz offset, 1 PERCH +50 DTCH, -37 dBc at 37 dBm average power) over the 2.5-2.7 GHz band. In this case Zout half the device was matched to 25-ohm impedance with a minimum loss and a return loss better than 20 dB. The full amplifier output matching circuit is shown figure 5C with the same remarks as for the input circuit concerning the lines and the capacitors.

Push-Pull Amplifier

The complete idealized amplifier schematic is shown in figure 5C.

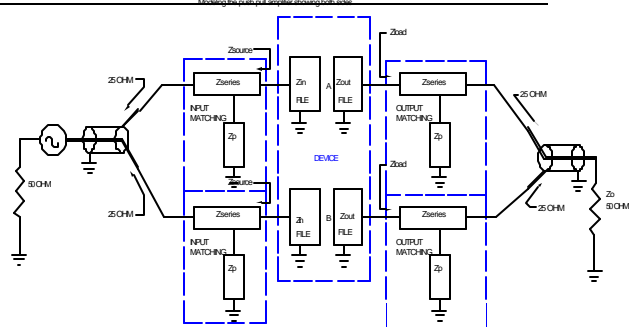


Figure 5B. Representation of Push-Pull matching showing complete circuit

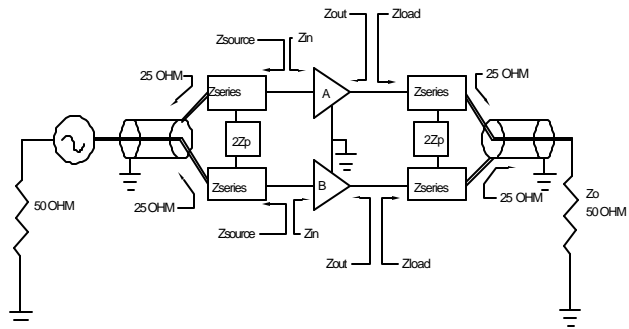


Figure 5C. The Final Schematic for a Push-Pull Amplifier

Large-Signal Circuit Tuning

To obtain optimum results, some tuning is usually necessary, in particular with respect to the output circuit. The reverse gain, S_{12} , of the FLL600IQ-3 60 Watt device is high enough to require re-tuning of the input circuit once the output match has been changed. The FLL600IQ-3 pre-matching and the parallel-line circuit topology of the amplifier make optimum tuning easy to achieve.

Note that tuning for optimum output power/power-added efficiency performance is different from that for WCDMA (Wideband Code Division Multiple Access) Adjacent Channel Power Ratio (ACPR) performance or for optimum IMD performance. Tuned input and output circuits for WCDMA ACPR performance are shown, Figures 7a and 7b.

Thermal considerations:

Device Maximum Power Dissipated Versus Flange Temperature

The maximum power dissipated, P_{diss.} by the device is limited by the maximum recommended channel temperature which is 175°C. It is important for the amplifier designer to be able to calculate the maximum P_{diss.} for their applications. This calculation is not as simple as it may appear since the thermal resistance of a GaAs device is a strong function of the device-flange temperature (T_f) and the channel temperature (T_{ch}) or P_{diss.}. The FLL600IQ-3 data sheet and the article “Understanding Thermal Basics For Microwave Power Devices”⁽³⁾ allow the designer to calculate the device thermal resistance (R_{th}) versus T_f and T_{ch} or P_{diss.}. It means by knowing R_{th1} for one set of the parameters (T_{f1} & T_{ch1}), R_{th2} can be calculated for another set of parameters (T_{f2}, T_{ch2} or P_{diss2}). The formulas are derived from the Kirchoff’s transformation and the variation of the GaAs thermal conductivity versus temperature. Because the flange thermal resistance (R_{thf}) is constant, it has to be subtracted from the global R_{th} before applying the correction.

We have assumed R_{thf}=0.3xR_{th}=0.24 K/W.

The initial values are from the device data sheet:

T_{f1}=25°C, T_{ch1}=25+0.8x12x4=63.4°C, R_{th}=0.8 K/W, R_{thf}=0.24 K/W

From these values, the maximum P_{diss.} can be calculated versus T_f for T_{ch}=175°C.

Table 3. Thermal Impedance and Max Power/Quiescent Current Example for R_{th} nominal = 0.8 K/W

T _f (°C)	T _{ch} (°C)	R _{th} (°K/W)	Max. P _{diss.} (W)	Max I _{dsq} at 12 V (A)
0	175	0.93	189.3	15.8
10	175	0.93	176.8	14.7
20	175	0.94	164.5	13.7
30	175	0.95	152.5	12.7
40	175	0.96	140.6	11.7
50	175	0.97	129.0	10.8
60	175	0.98	117.6	9.8
70	175	0.99	106.4	8.9
80	175	1.00	95.3	7.9
90	175	1.01	84.4	7.0
100	175	1.02	74.0	6.2

If the device is operated at low signal, the worst case is when there is no input signal and the above table gives I_{dsq} maximum versus T_f. If the device is operated only in compression then P_{diss.} maximum should be used and calculated with the following formula:

$$P_{diss.}=(V_{ds} \cdot I_{ds})+P_{in}-P_{out} \quad (W)$$

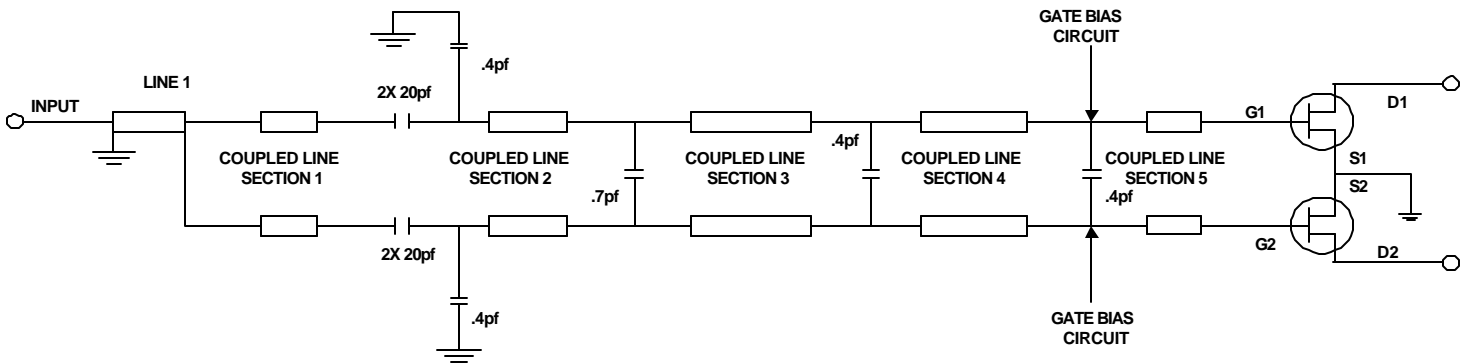
Device Attachment

Another thermal issue is the device attachment between the part flange and the housing. The device must be in good thermal contact with the heat sink.

A good heat exchanger to the ambient environment is also important but beyond the scope of this article.

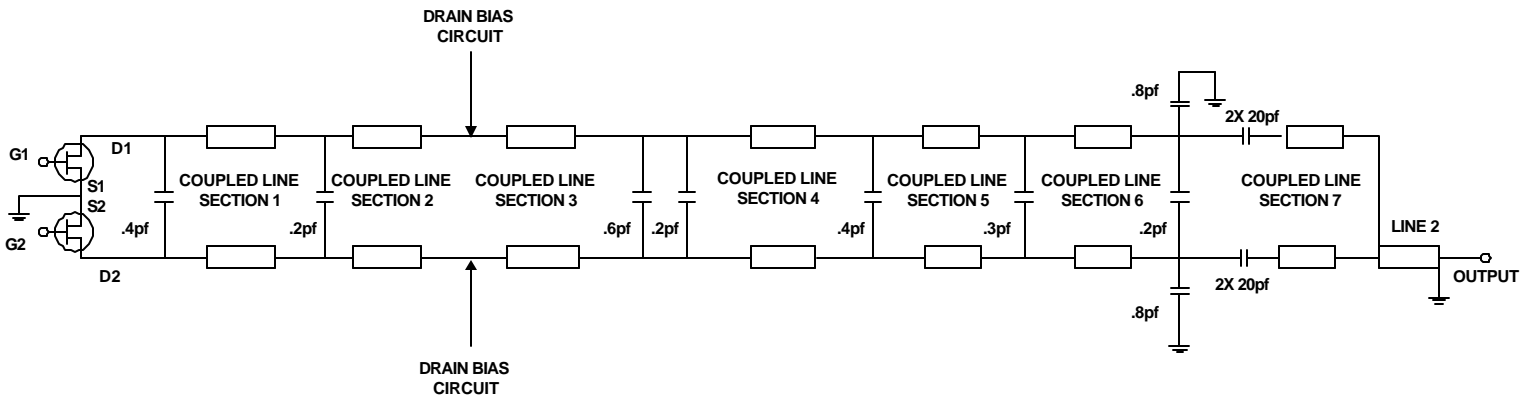
As each application has a unique set of system requirements relating to size, construction and environmental conditions, these parts of the thermal design are left to the user

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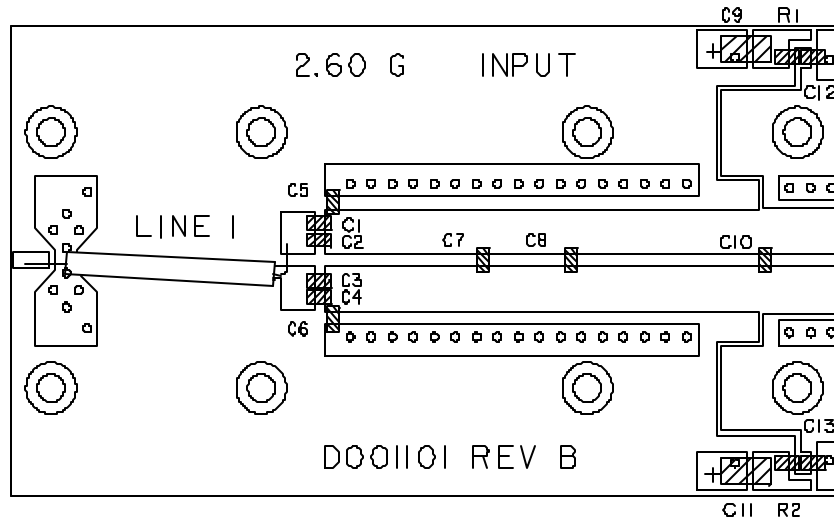
	W (mm)	S (mm)	L (mm)
Coupled line section 1	4.0	1.2	3.2
Coupled line section 2	4.2	1.2	15.0
Coupled line section 3	4.2	1.2	8.5
Coupled line section 4	4.2	1.2	18.4
Coupled line section 5	4.2	1.2	7.2

Figure 6A. Input matching network schematic for the 60W WCDMA amplifier using the FLL600IQ-3



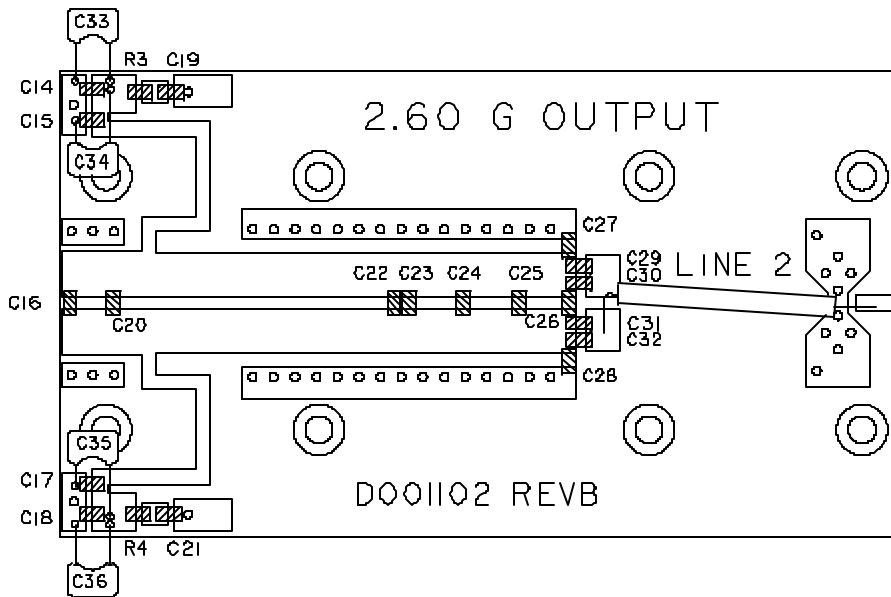
Coupled line section 1	4.2	1.2	4.8
Coupled line section 2	4.2	1.2	3.3
Coupled line section 3	4.2	1.2	23.7
Coupled line section 4	4.2	1.2	5.8
Coupled line section 5	4.2	1.2	5.2
Coupled line section 6	4.2	1.2	4.6
Coupled line section 7	4.0	1.2	3.2

Figure 6B. Output matching network schematic for the 60W WCDMA amplifier using FLL600IQ-3



REF DES	C1-C4	C5, C6, C8, C10	C7	C12-C13	C9, C11	R1, R2	LINE 1
VALUE	10pf	0.4pf	0.7pf	20pf	10uf	22 Ohm	
COMMENTS	Murata	Murata	Murata	Murata	Kemet	Rohm	24.5 mm

Figure 7a. Input Circuit for Optimum WCDMA ACPR Performance



REF DES	C33-C36	C14, C18	C20, C23, C26	C25	C16, C24	C22	C27, C28	C29-C32	C15, C17	C19, C21	R3, R4	LINE 2
VALUE	0.1uf	0.01uf	0.2pf	0.3pf	0.4pf	0.6pf	0.8pf	10pf	20pf	1000pf	51 Ohm	
COMMENTS	Kemet	Kemet	Murata	Murata	Murata	Murata	Murata	Murata	Murata	Murata	Rohm	24.5 mm

Figure 7b. Output Circuit for Optimum WCDMA ACPR Performance

Measured Results

The performance obtained with the FLL600IQ-3 using the circuitry of Figures 7a and 7b is presented in the following graphs. The amplifier was tuned for optimum WCDMA ACPR at 2600 MHz at a target average output power of 38 dBm with $V_{dsq} = 12V$ and $I_{dsq} = 4A$. No RF tuning changes were made for CDMA measurements at other I_{dsq} or those for IMD. The WCDMA signal source was an HP 4433B system, (WCDMA signal configuration -

4.096 MHz BW @ 5 MHz offset, 1 PERCH +

50 DTCH). ACPR was measured using HP8562A Spectrum Analyzer and 'Delta Marker Method' with a resolution bandwidth of 100 KHz and a video bandwidth of 100 Hz.

Figure 8 shows the output power versus input power. Figure 9 provides Power-Added Efficiency data vs. Power Output.

Figure 10 shows the output power versus frequency performance at various power levels.

Figure 11 shows WCDMA ACPR performance .

Figure 12 shows two CW tone intermodulation performance for the third order, fifth order, and seventh order products.

Figure 13 shows the Mean Time To Failure curve for the device type.

Conclusion

This application note provides the circuit designer with a design for a 60-W push-pull amplifier that can provide good WCDMA ACPR performance of -45 dBc

typical at output power levels of 6 W (38 dBm) for WCDMA base station applications.

Notes

(1): J. Shumaker, R. Basset and A. Skuratov, 'Power GaAs FET Amplifiers: Push-Pull versus Balanced Configuration', Wireless Symposium, 12-16 February 2001.

(2): R. Basset, "Three Balun Designs For Push-Pull Amplifiers", Microwaves, July 1980, page 47-52.

(3): R. Basset, "Understanding Thermal Basics For Microwave Power Devices", Microwaves & RF, October 2000, page 101-110.

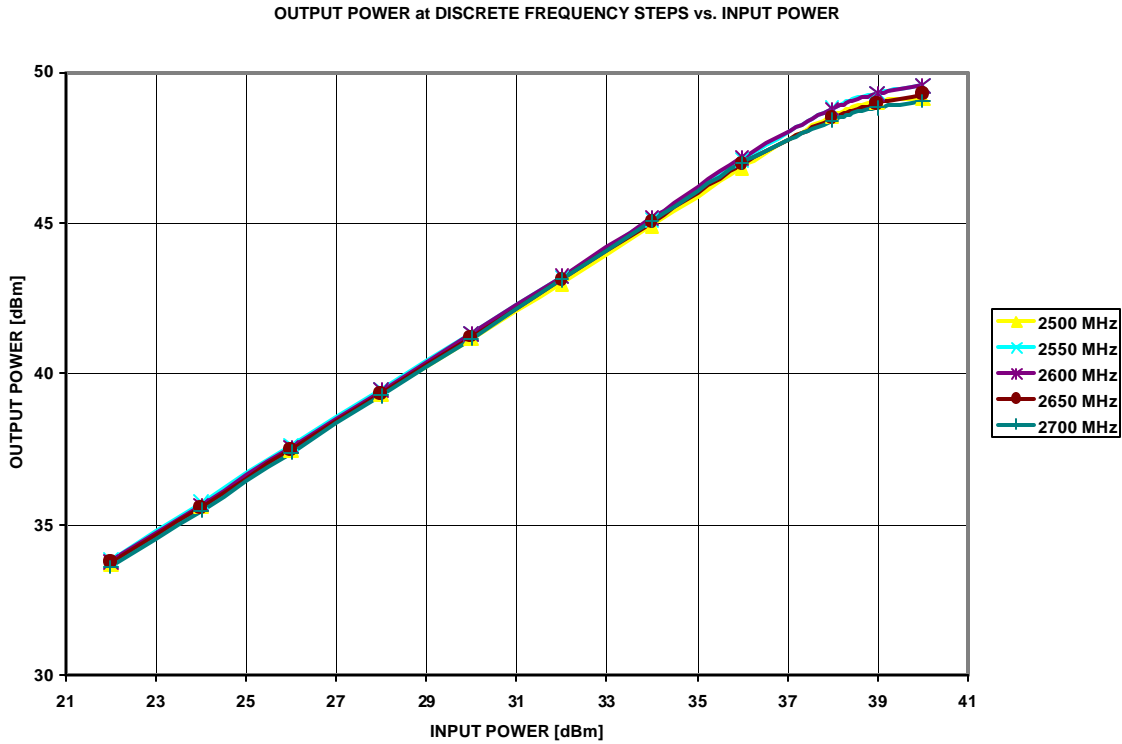


Figure 8. Output Power vs. Input Power at 2.5 to 2.7 GHz (tuned for WCDMA ACPR @ $I_{ds}=4A$)

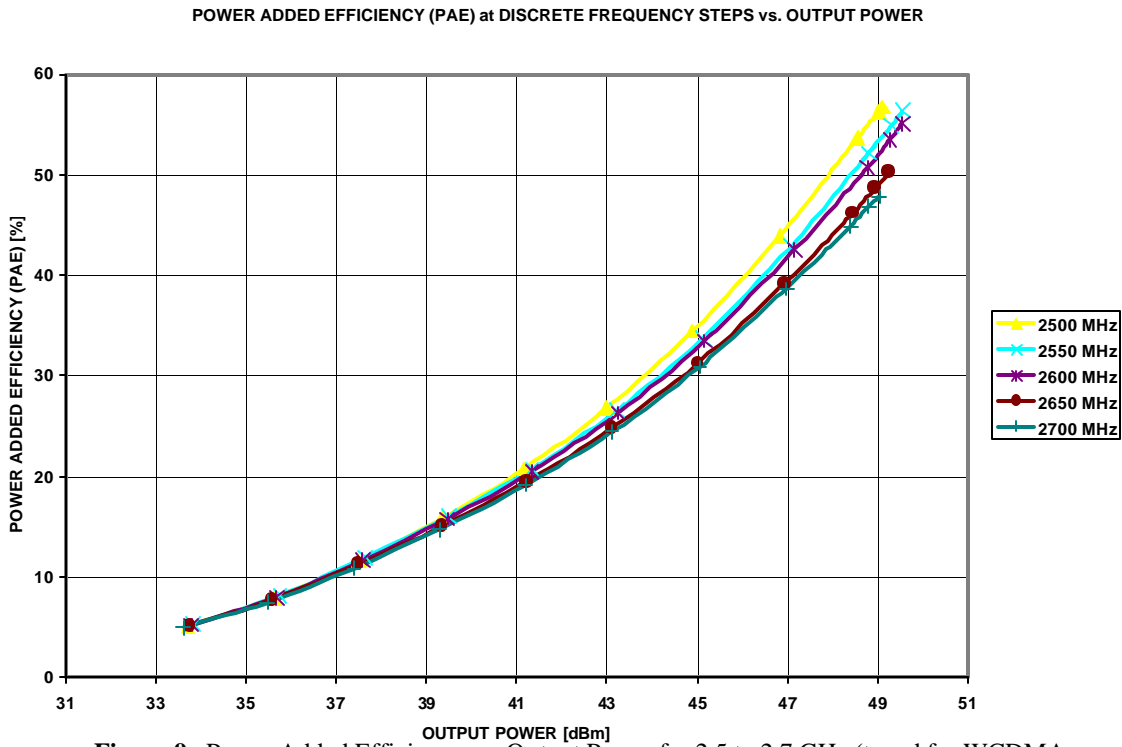


Figure 9. Power Added Efficiency vs. Output Power for 2.5 to 2.7 GHz (tuned for WCDMA ACPR @ $I_{ds}=4A$)

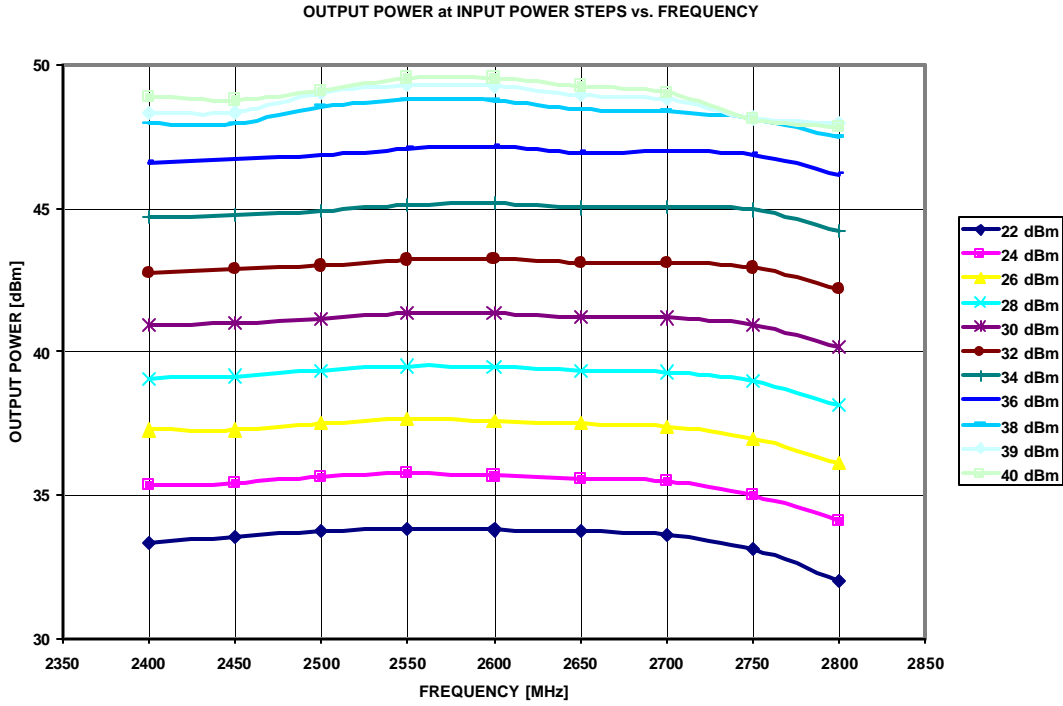


Figure 10. Power Output vs. Frequency for various Input Power Levels (tuned for WCDMA ACPR @ $I_{ds}=4A$)

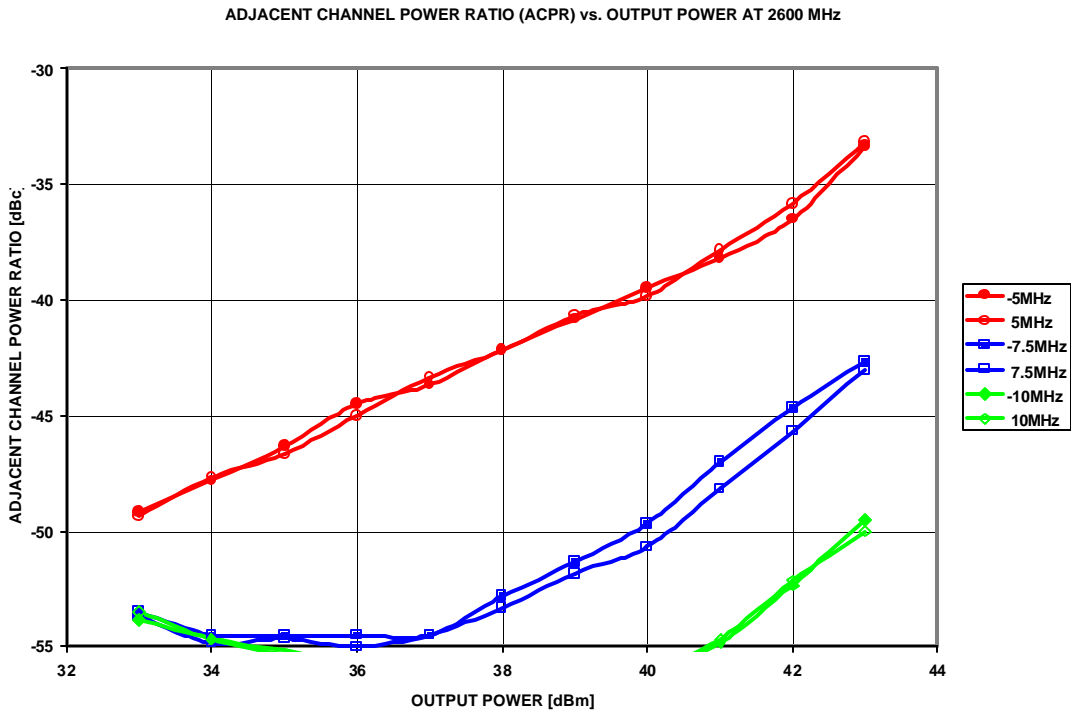


Figure 11. Adjacent Channel Power vs. Output Power at 2.6 GHz (tuned for WCDMA ACPR @ $I_{ds}=4A$)

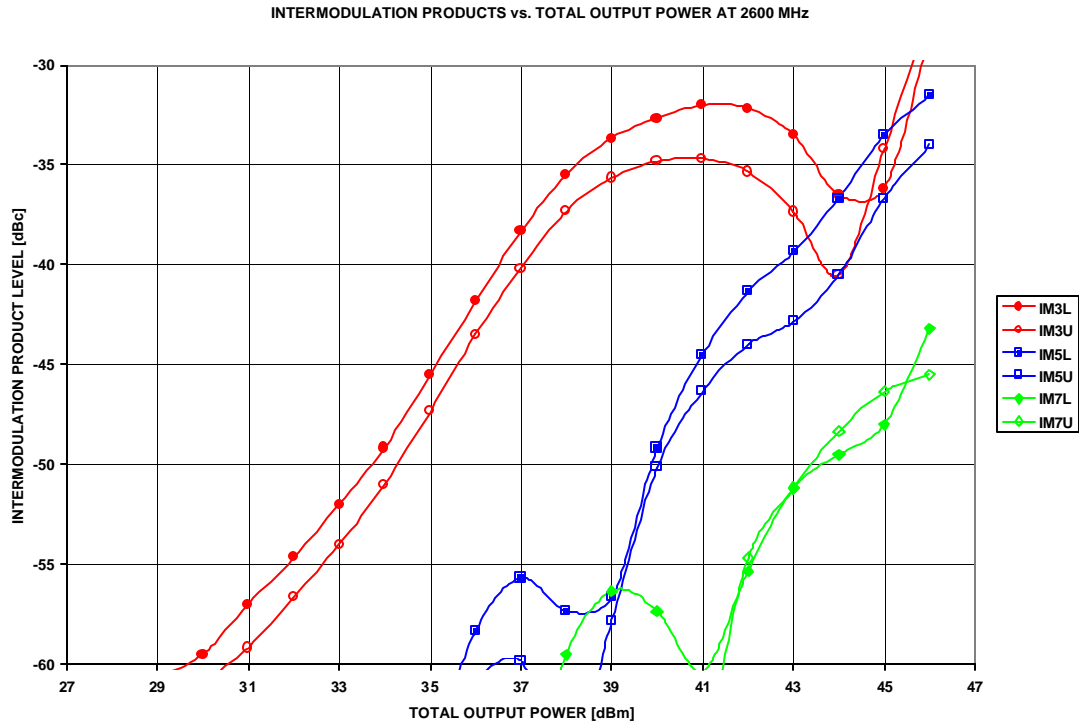


Figure 12. Intermodulation Products vs Output Power at 2.6 GHz (tuned for WCDMA ACPR @ $I_{ds}=4A$)

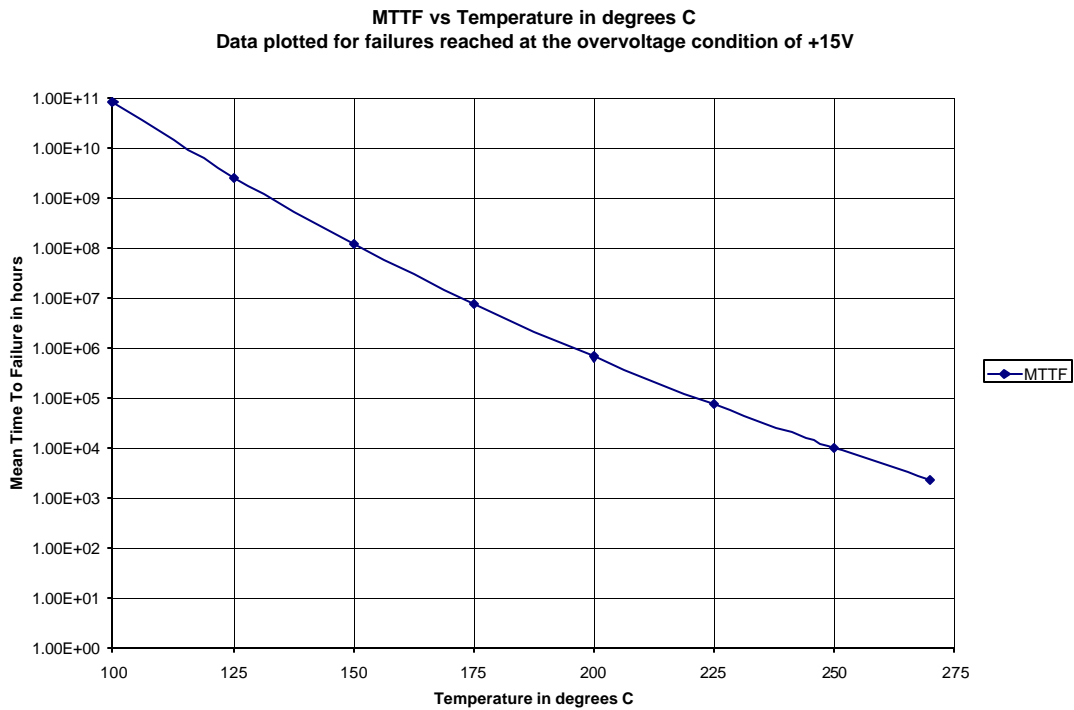


Figure 13. MTTF vs junction temperature in degrees C. The data is for 15Volt drain bias, an overvoltage condition. 12V testing has reached no failures, so actual reliability is higher than the curve shown.

FLL600IQ-3 Device Data

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta=25°C)

Parameter	Symbol	Condition	Rating	Unit
Drain Source Voltage	V _{DS}		15	V
Gate-Source Voltage	V _{GS}		-5	V
Total Power Dissipation	P _T	T _c = 25°C	125	W
Storage Temperature	T _{stg}		-65 to +175	°C
Channel Temperature	T _{ch}		+175	°C

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs :

1. The drain-source operating voltage (V_{DS}) should not exceed 12 volts.
2. The forward and reverse gate currents should not exceed 117mA and -35.4mA respectively with gate resistance of 10W

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Drain Current	I _{DSS}	V _{DS} = 5V, V _{GS} = 0V	-	21	32	A
Pinch-Off Voltage	V _p	V _{DS} = 5V, I _{DS} =1.44A	-1.0	-2.0	-3.0	V
Gate-Source Breakdown Voltage	V _{GSO}	I _{GS} = -1.44 mA	-5	-	-	V
Output Power	P _{out}	V _{DS} = 12V F=2.17 GHz I _{DS} = 4A Pin=39.0 dBm	47.0	48.0	-	dBm
Linear Gain	GL		9.0	10.0	-	dB
Drain Current	I _{DSR}		-	11.0	15.0	A
Power-Added Efficiency	h _{add}		-	43	-	%
Thermal Resistance	R _{th}		Channel to case	-	0.8	1.2

Case Style "IQ"

