FUJITSU APPLICATION NOTE - No 002

1930MHz - 1990 MHz PCS BASE STATION APPLICATIONS

40 Watt Push-Pull Amplifier using the FLL400IP-2 GaAs FET

FEATURES

- Meets CDMA ACP at Pout>8W
- Over 40 W P_{1dB} over entire PCS band
- High gain / high PAE
- Excellent reproducibility
- Easy tuning for Power, IM3 or CDMA ACP
- Over 10:1 VSWR without damage
- Very high MTTF : $>10^8$ hours
- High linearity means low cost per Watt

SUMMARY

A 40 Watt push-pull amplifier design for the 1930-1990MHz PCS band using the Fujitsu FLL400IP-2 GaAs FET is presented. Full circuit design details as well as the measured results for both Class A and AB operation are provided.

Circuit Description

The circuitry described in this application note provides the RF engineer with a straight-forward, robust design for a 40 Watt push-pull amplifier. Due to the inherent linearity of the push-pull configuration, this design is ideally suited for PCS applications requiring high linearity and efficiency. The high linearity is obtained with a minimum of components and tuning and can operate over the entire 1930-1990 MHz PCS band. Acceptable CDMA ACP performance has been obtained at

6 W output power.

Push-Pull Circuit Advantages

Devices operating in the push-pull configuration have several inherent advantages over single-ended Class A operated devices. These include:

- better power-added efficiency
- easier matching, since two smaller gate devices are used in series
- push-pull symmetry which minimizes even-order distortion products

Fujitsu has specifically designed the FLL400IP-2 to significantly reduce odd-order distortion products by utilizing the FET linearity and an internal matching network. The FLL400IP-2 is equivalent in linearity to much higher power single-ended devices.

40 Watt PCS Amplifier Components

The RF circuit elements of the 40W amplifier are the Fujitsu FLL400IP-2, 40W power GaAs FET, two SHOSHIN balun chips and several capacitors and resistors mounted on a dielectric substrate. A detailed parts list can be found in Figure 7.

FLL400IP-2 Device Description

The FLL400IP-2 utilizes a pair of 20 Watt Au gate power GaAs FETs that are DC and RF connected in a push-pull configuration within the Fujitsu IP package. Impedance matching networks are used within the package to raise the input and output impedances to allow for easier circuit board tuning. The 0.8μm Au gate FETs have an MTTF of greater than 10^8 hours for a channel temperature of 125°C.

The transistor chips and the IP package have been optimized for extremely low thermal resistance, typically 1.2 °C/W. Additionally, the IP package is hermetically sealed for applications where extreme environments may be encountered.

Balun and Board Material Description

The compact 1930MHz - 1990MHz 40 Watt linear amplifier design presented in the following sections is achieved by using SOSHIN GSC371-BAL2000 balun chips and a Rogers RO3010 high dielectric constant (ε_r) substrate. All components used in the design are commercially available. The substrate's physical and electrical parameters are summarized below. If small size is not critical, a lower dielectric constant board material can be used with no performance degradation.

ε_r	h, mm	Metallization	thickness
10.2	0.635	Cu	17μm

Rogers RO3010 substrate parameters

DC Bias Circuit Topology

When using power GaAs FETs, it is necessary to take into account the following aspects of device operation : low frequency instability, very high out-of-band VSWRs and the necessity of limiting forward gate current when the device is operating under high RF drive levels.

Low Frequency Instability

The high out-of-band VSWRs along with the high gain and output power of the power GaAs FET induces instability at low frequencies. This can show up in the form of large low frequency oscillations which can destroy the device. The rugged construction of the FLL400IP-2 device and internal matching reduce this possibility. It is, however, important to take some basic precautions.

The first elementary precaution is to properly decouple the gate and drain bias networks. This must be done in several frequency ranges. To counter very low frequency instability, it is necessary to use high value 10μF miniature tantalum capacitors. In the HF frequency range, 0.1µF ceramic chip or radial mono capacitors can be used. Finally for VHF/UHF decoupling 1000pF ceramic chip capacitors are adequate.

Out-of-Band Damping

Resistive damping networks are generally used to ensure that the device is properly terminated at out-of-band frequencies. This is particularly important in the case of circuits using baluns, as the latter are often highly reactive at out-of-band frequencies.

The simplest damping circuit for narrow band amplifiers comprises a quarter-wavelength high impedance line transformer terminated with an RF short circuited resistor as shown in Figure 1.

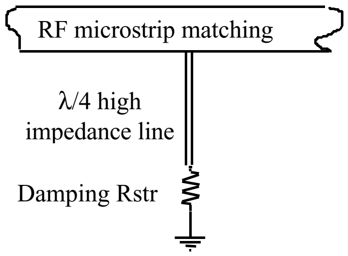


Figure 1. Typical damping circuit

At in-band frequencies, the quarter-wavelength high impedance transmission line ensures that the resistor will not affect circuit performance. At out-of-band frequencies the network damps gain and offers resistive matching, thereby contributing to stability from oscillation.

By placing this damping circuit close to the transistor, we can also use it as a bias network and an RF pre-matching element. Thereby combining three functions in one circuit.

Forward Gate Current Protection

Under large signal drive conditions, the Schottky-barrier gate diode of the GaAs FET will be driven into forward conduction. If the associated current is too high, the accompanying thermal effect gradually alloys the gate junction and degrades transistor action. To limit gate diode current under RF voltage drive, it is customary to use a series resistor in the gate bias circuit. An increase in current leads to an increase in the voltage drop across the resistor thus limiting the voltage swing at the gate. The resistor value must be carefully chosen. Too large a resistance will diminish amplifier power-added efficiency by limiting RF voltage excursion. Too small a value will lead to long term degradation of the transistor and reduced MTTF. The optimum gate series resistance for the FLL400IP-2 is 50 Ohms, limiting gate current to the rated 16mA.

The bias networks shown in Figures 2 and 3 utilize the techniques described above. The circuit board layouts are included in Figures 7a and 7b.

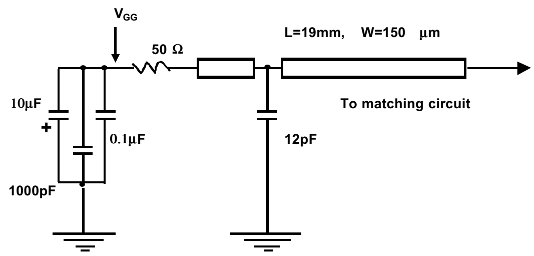
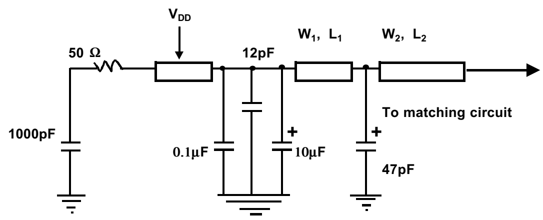


Figure 2. Gate bias network



W_1 (µm)	L_1 (mm)	W_2 (µm)	L_2 (mm)
540	4.4	540	4.4

Figure 3. Drain bias network

RF Matching with Push-Pull Devices

FLL400IP-2 RF Parameters

The PCS frequency band conjugate source and load impedances for optimum CDMA ACP performance are provided in the following table. The bias conditions associated with these impedances are V_{DS} = 12V and I_{DS} = 2A.

Frequency	Z_L*(Ohm)		Z_S*(Ohm)	
MHz	Real	Imag.	Real	Imag.
1930	9	-17.2	35	-109
1960	8.5	-17.2	32.5	-100
1990	8	-17.2	31.5	-92

40 W Optimum Conjugate Source and Load Impedances

Use of Optimum Load Impedances

Matching push-pull devices to their optimum impedances is best understood by considering Figures 4a and 4b.

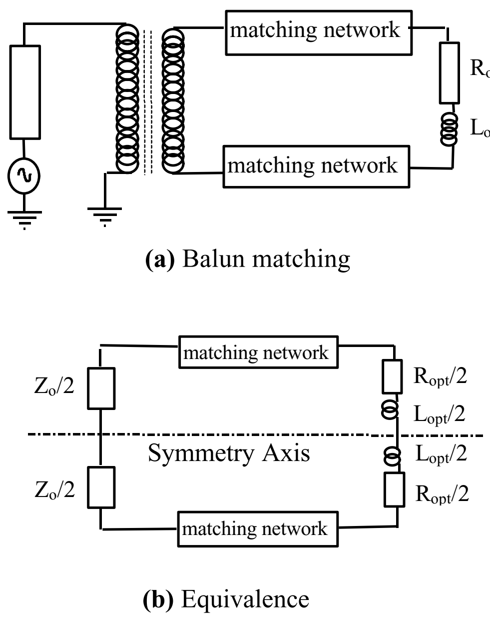


Figure 4. Representation of Push-Pull matching

In the design example presented in the following section, we shall use a coupled-line matching topology for the input and output RF matching circuits. In this case, Figure 4b applies. For simulation, we match to half the optimum load impedance in each coupled-line branch.

Circuit Design and Simulation

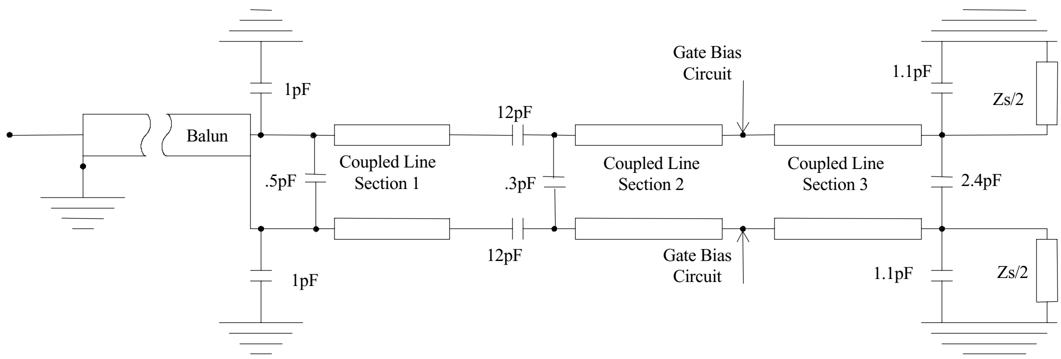
For the purposes of simulation, the SOSHIN balun chip is represented as a classical quarter-wave transmission line balun. In-band behavior of the chip balun is very similar to that of the transmission-line balun, so the approximation is good for the simulation. Out-of-band behavior is quite different, however, so careful attention must be paid to suppress spurious oscillations caused by chip balun resonances.

Quarter-wavelength coupled-line transformers are used to match the balun output impedance, Z_0 /2, to the conjugate of half the optimal impedance, $Z_s^*/2$, in the case of input match, and $Z_L^*/2$ in the case of output match. The input matching network schematic is given in Figure 5. The output matching network schematic is given in Figure 6.

Large-Signal Circuit Tuning

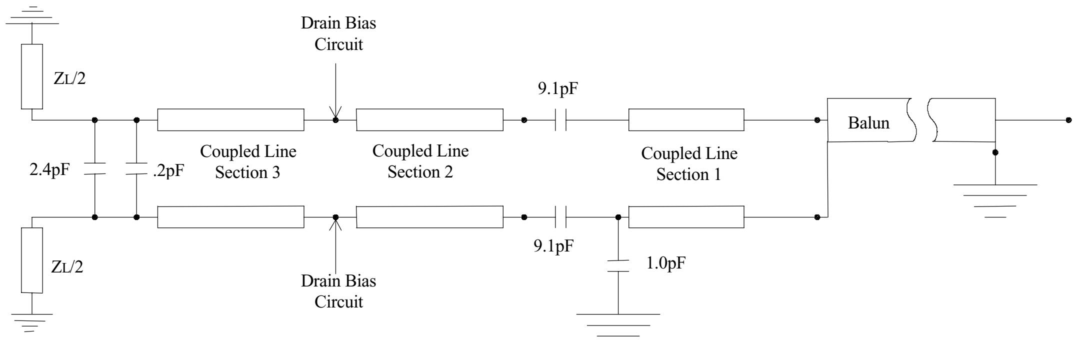
To obtain optimum results, some re-tuning is necessary, in particular with respect to the output circuit. The reverse gain, S_{12} , of the FLL400IP-2 40Watt device is high enough to require re-tuning of the input circuit once the output match has been changed. The FLL400IP-2 pre-matching and the coupled-line circuit topology of the amplifier make optimum tuning easy to achieve, however.

Note that tuning for optimum output power/power-added efficiency performance is different from that for CDMA (Code Division Multiple Access) Adjacent Channel Power (ACP) performance or for optimum IMD performance. Tuned input and output circuits for CDMA ACP performance are shown, Figures 7a and 7b.



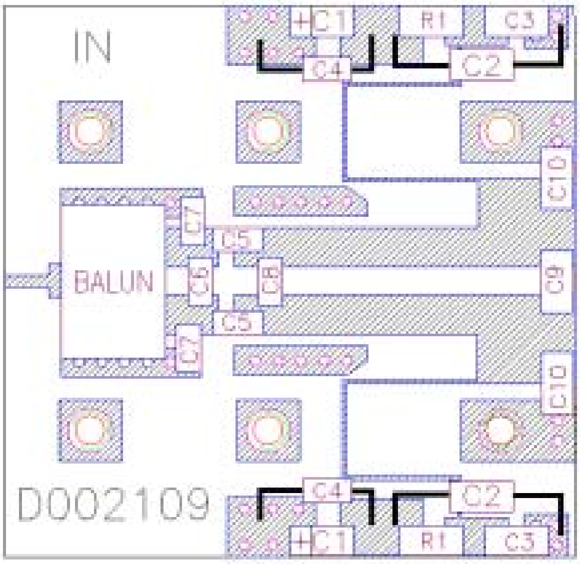
	W (mm)	S (mm)	L (mm)
Coupled line section 1	1.9	1.42	3
Coupled line section 2	1.9	1.42	11.725
Coupled line section 3	4.36	1.42	4.773

Figure 5. Input matching network schematic for the 40WPCS Amplifier using the FLL400IP-2



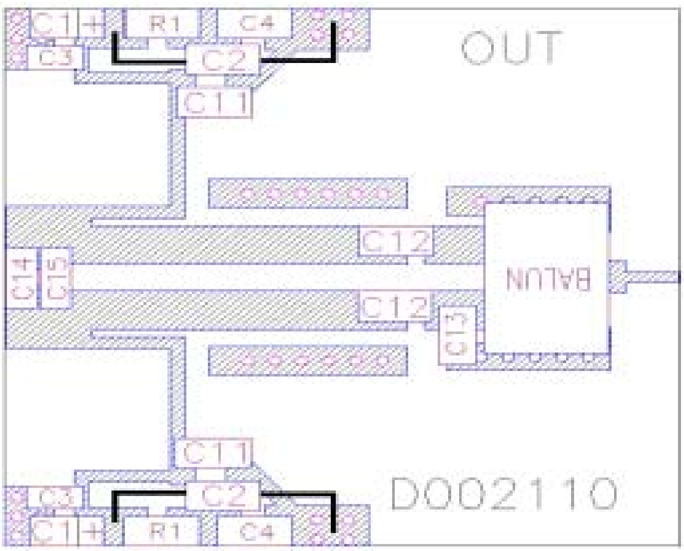
	W (mm)	S (mm)	L (mm)
Coupled line section 1	1.9	1.42	3
Coupled line section 2	1.9	1.42	12.913
Coupled line section 3	2.87	1.42	3.471

Figure 6. Output matching network schematic for the 40W PCS amplifier using FLL400IP-2



C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	R1
10µF	0.1µF	12pF	1000pF	12pF	0.5pF	1pF	0.3pF	2.4pF	1.1pF	50Ω
Tant	Ceramic Dipped	Murata	Murata	ATC	Soshin	Soshin	ATC	ATC	Soshin	ROHM

Figure 7a. Input Circuit for Optimum CDMA ACP Performance



C1	C2	C3	C4	C11	C12	C13	C14	C15	R1
10µF	0.1µF	12pF	1000pF	47pF	9.1pF	1pF	2.4pF	0.2pF	50Ω
Tant	Ceramic Dipped	Murata	Murata	Murata	ATC	Soshin	ATC	ATC	ROHM

Figure 7b. Output Circuit for Optimum CDMA ACP Performance

Measured Results

The performance obtained with the FLL400IP-2 using the circuitry of Figures 7a and 7b is presented in the following graphs. The amplifier was tuned for optimum CDMA ACP at 1960 MHz at a target output power of 37.5 dBm with Vdsq = 12V and Idsq=2A. No RF tuning changes were made for CDMA measurements at other bias settings or those for IMD. The CDMA signal source was an HP MCSS system, 64 channel enabled. ACP was measured using the ' Delta Marker Method' with a resolution bandwidth of 30 KHz and a video bandwidth of 100 Hz.

Figure 8 shows the frequency response of the amplifier design. Figure 9 gives the output power and power added efficiency performance versus input power. Figures 10-12 provide CDMA ACP data for three different bias points. The circuitry was tuned with Vds=12V, Ids=2A. Only the bias was adjusted for Figures 11 and 12. ACP performance is not markedly different between the three biases. Similarly, Figures 13 – 15 provide the IMD performance of the amplifier for the three different bias points. With this data, it is apparent that IMD is improved with the higher Idsq biasing even with the RF tuning fixed. This, however, is at the cost of efficiency.

In order to provide the optimum performance for a specific bias point, the RF tuning may need to be adjusted. The antenna interface impedance will also necessitate tuning adjustments.

Heatsinking

Although a thermal design procedure was not specifically addressed in this application note, it plays a crucial part in the reliable operation of the power amplifier. As each application has a unique set of system requirements relating to size, construction and environmental conditions, the thermal design is left to the user.

Conclusion

This application note has provided the circuit designer with a straightforward design for a 40W push-pull amplifier that can provide acceptable CDMA ACP perfomance at output power levels up to 8 watts.

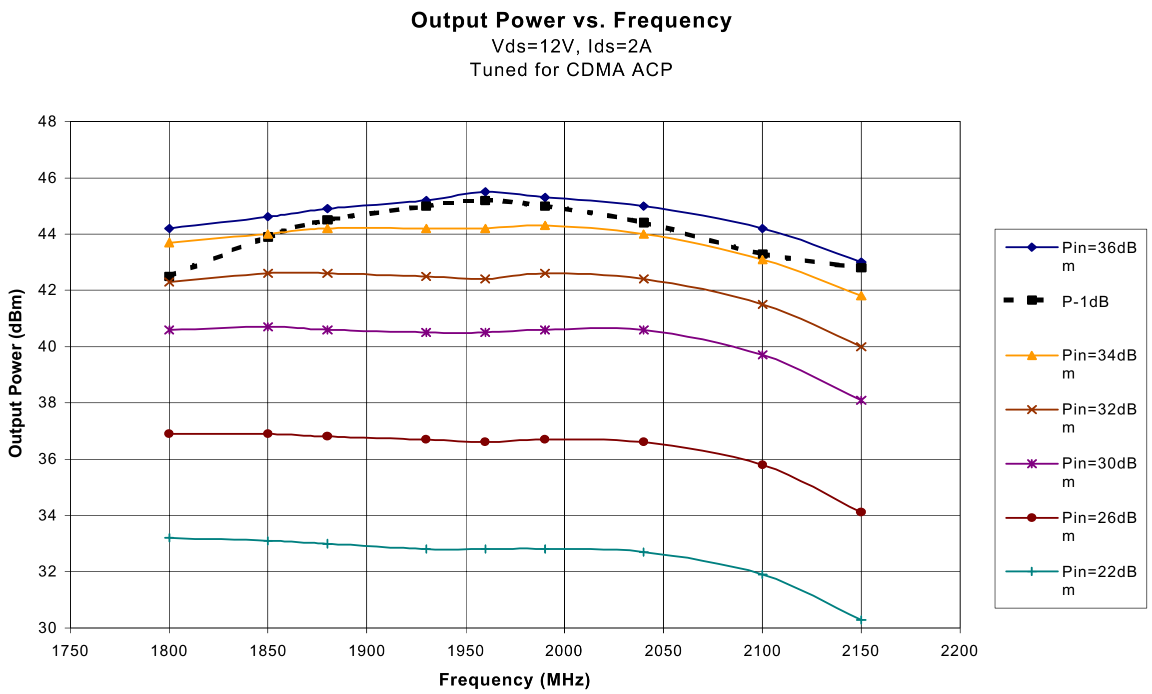


Figure 8. Output Power versus Frequency

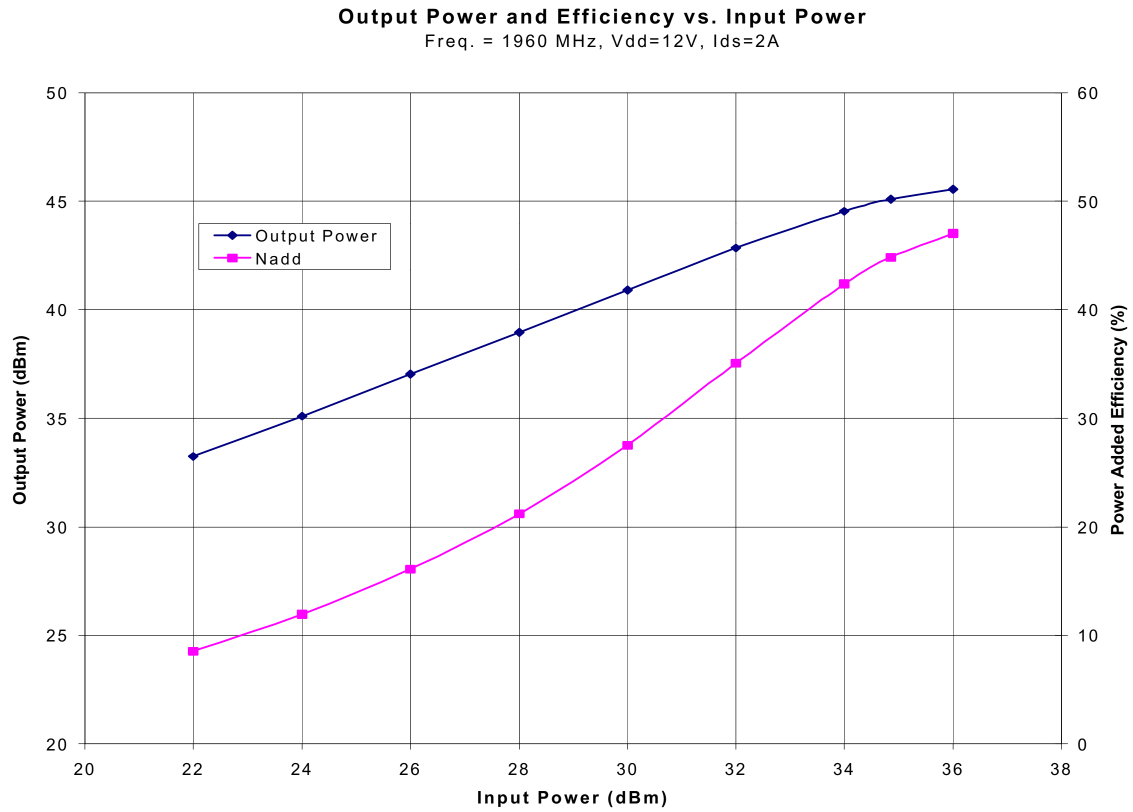


Figure 9. Output Power and PAE vs. Input Power

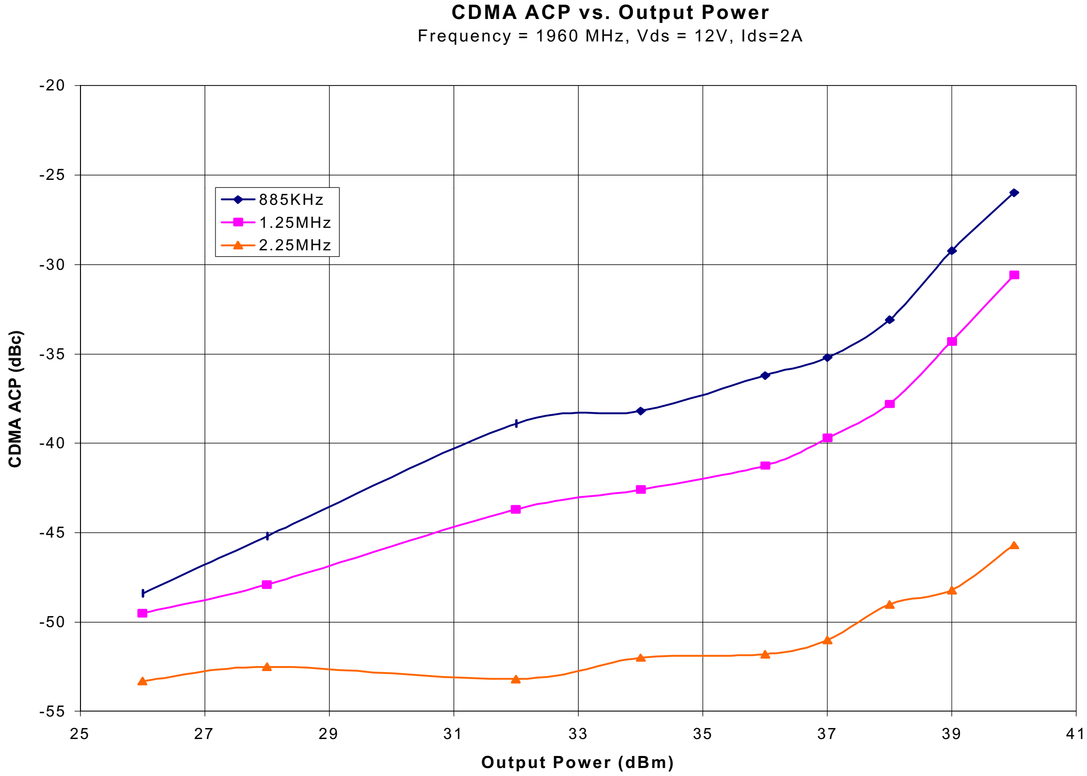


Figure 10. CDMA ACP versus Output Power (12V,2A)

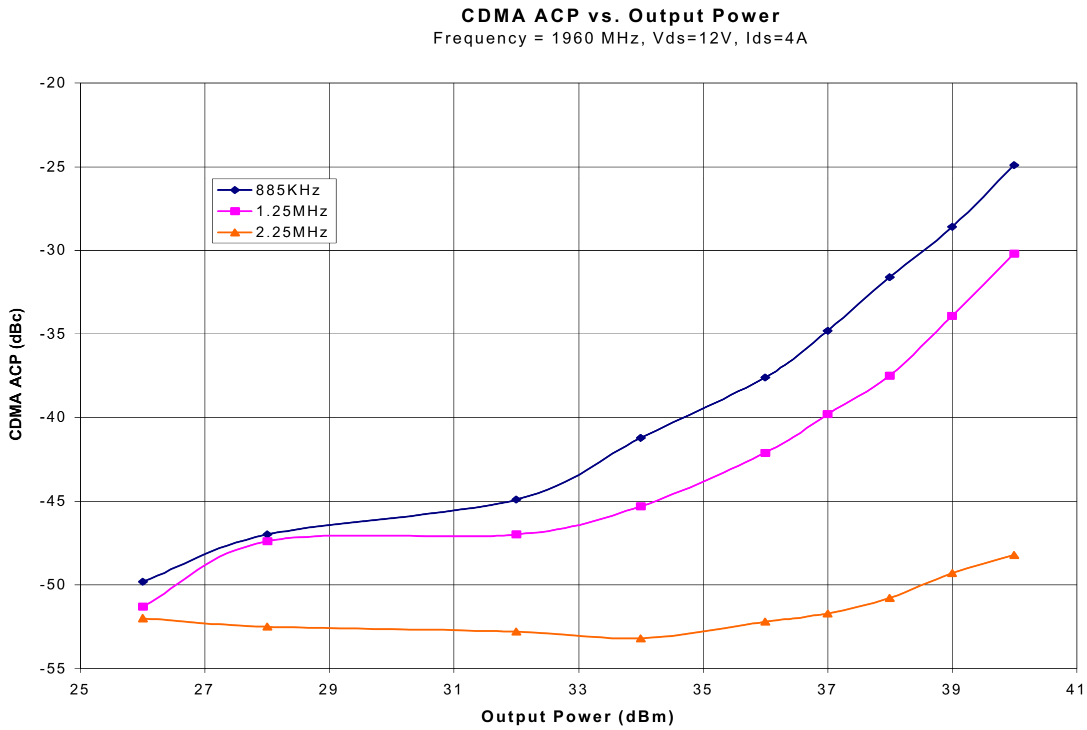


Figure 11. CDMA ACP versus Output Power (12V, 4A)

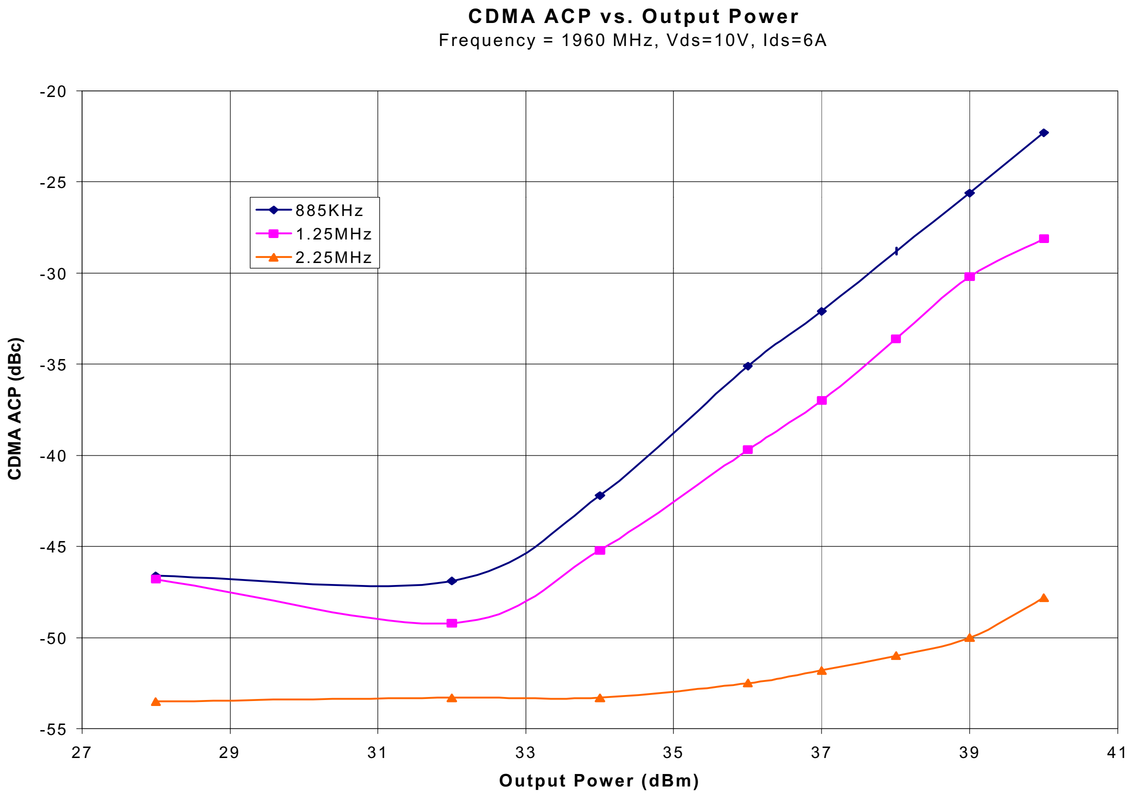


Figure 12. CDMA ACP versus Outpur Power (10V, 6A)

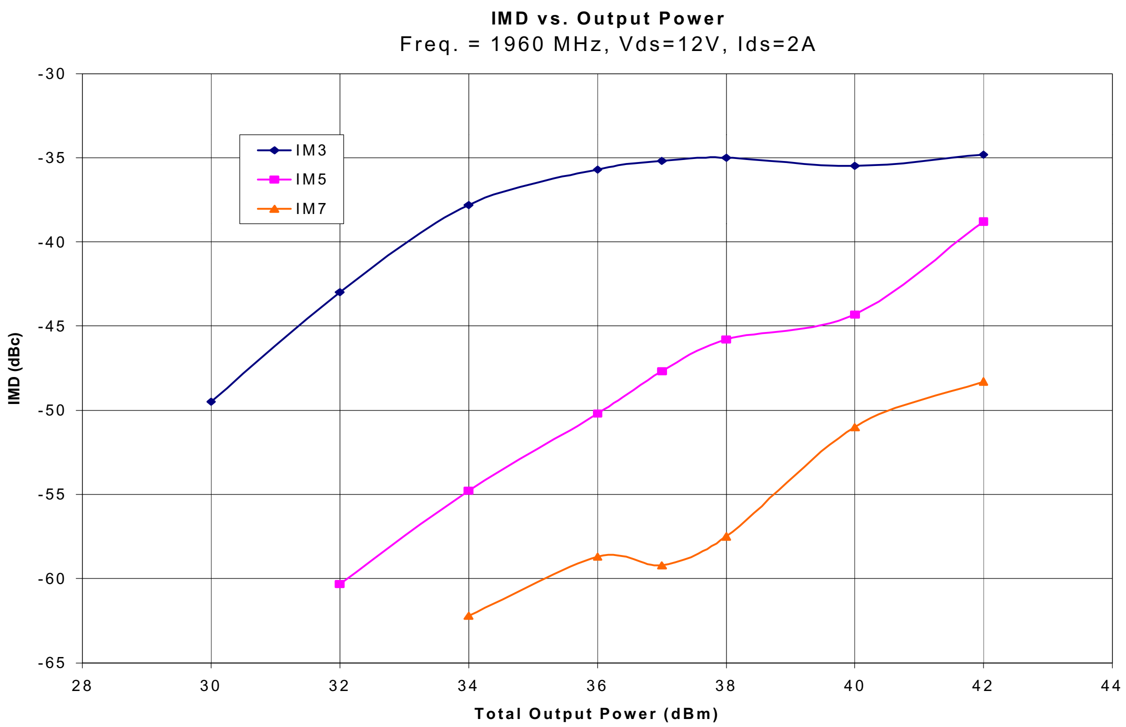


Figure 13. IMD versus Output Power (12V,2A)

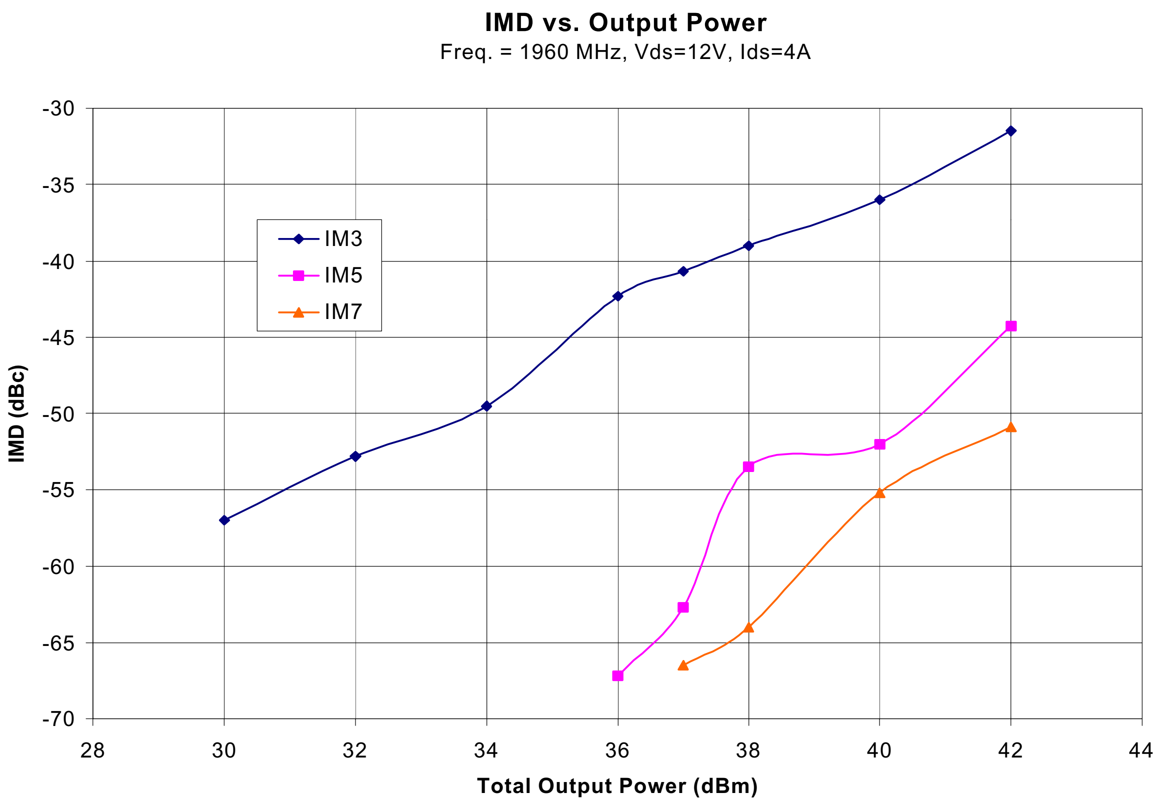


Figure 14. IMD versus Output Power (12V, 4A)

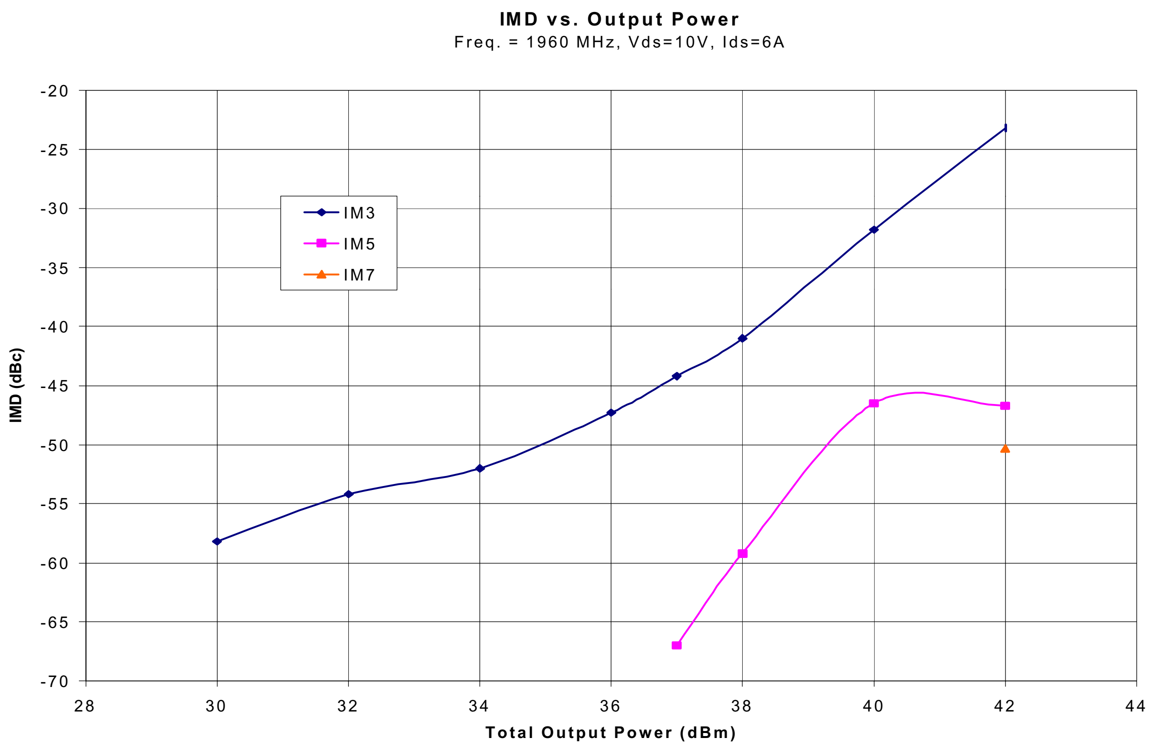


Figure 15. IMD versus Output Power (10V, 6A)

FLL400IP-2 Device Data

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta=25°C)

Parameter	Symbol	Condition	Rating	Unit
Drain Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T	Tc = 25°C	93.7	W
Storage Temperature	T_{stg}		-65 to +175	°C
Channel Temperature	T_{ch}		+175	°C

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs :

1, The drain-source operating voltage (V_{DS}) should not exceed 12 volts.
2. The forward and reverse gate currents should not exceed 54.4mA and –-17.4mA respectively with gate resistance of 25Ω

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0V	-	12	16	A
Transconductance	gm	V_{DS} = 5V, I_{DS} = 7.2A	-	6000	-	mS
Pinch-Off Voltage	V_p	V_{DS} = 5V, I_{DS} = 720mA	-1.0	-2.0	-3.5	V
Gate-Source Breakdown Voltage	V_{GSO}	I_{GS} = -720μA	-5	-	-	V
Output Power at 1 dB G.C.P.	P_{1dB}	V_{DS} = 12V	44.5	45.5	-	dBm
Power Gain at 1 dB G.C.P.	G_{1dB}	F=1.96GHz	9.0	10.0	-	dB
Drain Current	I_{DSR}	I_{DS} = 2.0A	-	6.0	8.0	A
Power-Added Efficiency	η_{add}	Note 1	-	44	-	%
Output Power at 1 dB G.C.P.	P_{1dB}	V_{DS}=10V f=1.96GHz	-	44.5	-	dBm
Power Gain at 1 dB G.C.P.	G_{1dB}	I_{DS}=5A	-	10.0	-	dB
Thermal Resistance	R_{th}	Channel to case	-	1.0	1.4	°C/W

CASE STYLE : IP

G.C.P. : Gain Compression Point

Note 1 : The device shall be measured at a constant V_{GS} condition.